EVAL_100W_DRIVE_CFD2

100 W motor drive evaluation board with FOC sensorless control

About this document

This application note provides an overview of the evaluation board EVAL_100W_DRIVE_CFD2, including its main features, key data, pin assignments, schematics and layout. It also describes how to quickly get started with this demo PCB and take advantage of Infineon's CoolMOS CFD™ Superjunction (SJ) MOSFETs, CoolSET™ quasi resonant (QR) flyback controller and XMC1000 series microcontroller.

EVAL_100W_DRIVE _CFD2 is a 100 W motor drive evaluation board with FOC sensorless control, which demonstrates Infineon's CoolMOS™ technology for motor drives by introducing a complete system-level solution using discrete inverter solution to control and drive three-phase motors.

The evaluation board EVAL_100W_ DRIVE _CFD2 for motor drive applications was developed to support customers in the first steps of designing applications with discrete solutions.

Scope and purpose

To demonstrate the efficiency of the evaluation board and present a thermal solution for the inverter stage with Infineon's CoolMOS™ CFD SJ MOSFETs. Also to show the algorithm control and help reduce reverse-current hard-commutation stress by offering a synchronous rectification (SR) algorithm to a sensorless field-oriented BLDC/PMSM control (FOC) with feedback (FB) current loop, by using the XMC1000 series microcontroller. This enables manufacturers to minimize time-to-market and also reduces the size of the Bill of Materials (BOM).

The Infineon components used in the 100 W motor drive evaluation board are:

- IFX1763XEJ V50 low drop-out voltage regulator
- IPD65R1K4CFD 650 V CoolMOS™ CFD MOSFET
- 2EDL05N06PF 600 V half-bridge gate driver IC with LS-SOI technology (EiceDRIVER™)
- BSS314PE P-channel small-signal MOSFET
- BSS138N N-channel small-signal MOSFET
- BAT54-03W silicon Schottky diode
- XMC1302-T038X0200 microcontroller
- ICE5QR4770AG CoolSET™ Quasi Resonant QR Flyback controller

Intended audience

This application note is intended for all technical specialists who aim to reduce system cost and improve efficiency, which in turn will enable longer run-time and reduce time-to-market.

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1 Safety precautions

In addition to the precautions listed throughout this manual, please read and understand the following statements regarding hazards associated with development systems.

Table 1 Precautions

	**Attention:** The ground potential of the EVAL_100W_DRIVE_CFD2 system is biased to a negative DC bus voltage potential. When measuring voltage waveform by oscilloscope, the scope's ground needs to be isolated. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.
	**Attention:** Only personnel familiar with the drive and associated machinery should plan or implement the installation, start-up and subsequent maintenance of the system. Failure to comply with this may result in personal injury and/or equipment damage.
	**Attention:** The surfaces of the drive may become hot, which may cause injury.
	**Attention:** The EVAL_100W_DRIVE_CFD2 system contains parts and assemblies sensitive to Electro Static Discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing this assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to applicable ESD protection handbooks and guidelines.
	**Attention:** A drive, incorrectly applied or installed, can result in component damage or reduction in product lifetime. Wiring or application errors such as under-sizing the motor, supplying an incorrect or inadequate AC supply or excessive ambient temperatures may result in system malfunction.
	**Attention:** Remove and lock out power from the drive before you disconnect or reconnect wires or perform a service. Wait three minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.
	**Attention:** The EVAL_100W_DRIVE_CFD2 system contains DC bus capacitors which take time to discharge after removal of the mains supply. Before working on the drive system, wait three minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.

2 Introduction

The EVAL_100W_DRIVE_CFD2 evaluation board is available from Infineon. The features of this board are described in the design features section of this document, while the remaining paragraphs provide information to enable users to copy, modify and qualify the design for production according to their own specific requirements.

The EVAL_100W_DRIVE_CFD2 evaluation board uses the µC/Probe™ XMC™ platform. µC/Probe™ XMC™ is a Windows-based application that allows you to read and write the memory of XMC™ microcontrollers during run-time in a non-intrusive way, with a graphical dashboard to enable visualization of real-time data of critical control loops in motor control and fine-tune your motor parameters to meet target applications.

This board can be easily interfaced through XMC™ Link. XMC™ Link is an isolated debug probe for all XMC™ microcontrollers. The debug probe is based on SEGGER J-Link debug firmware, which enables use with DAVE™ and all major third-party compiler/IDEs known from the wide ARM® ecosystem.

This evaluation board is designed to give a complete solution for sensorless motor drives, using CoolMOS™ technology as a discrete solution for the power stage .The board is equipped with all assembly groups for sensorless Field Oriented Control (FOC). It provides a single-phase AC connector, rectifier, QR controller CoolSET™ for bias circuit, DC-link and three-phase output for power. It contains emitter-shunts for current sensing (CS) and a voltage divider for DC-link voltage measurement.

2.1 Description

The EVAL_100W_DRIVE_CFD2 motor drive demo board comes with AC input voltage and a 100 W max. output power to drive a three-phase BLDC/PMSM motor with FOC sensorless mode suited to fridge, fan and pump applications, due to the CoolMOS™ CFD and XMC1000 microcontroller used inside this board.

This board does not only offer a synchronous rectification (SR) algorithm to reduce reverse-current hard-commutation stress and sensorless field-oriented BLDC/PMSM control (FOC), but also this algorithm gives the user the option to change switching frequency and choose between two-phase or three-phase modulation (seven-segment space-vector modulation (SVM) or five-segment SVM) which helps to reduce switching losses, reduce the platform EMI and improve total efficiency, resulting in reliable and compact system designs. The BOM is minimized due to copper area reduction, while meeting the minimum requirements for target applications.

2.2 Summary of features

- Low BOM cost due to the CoolMOS™ CFD and XMC™ algorithm
- Highly efficient solution
- Sensorless field-oriented BLDC control (FOC)
- Ease of use with graphical user interface (GUI)

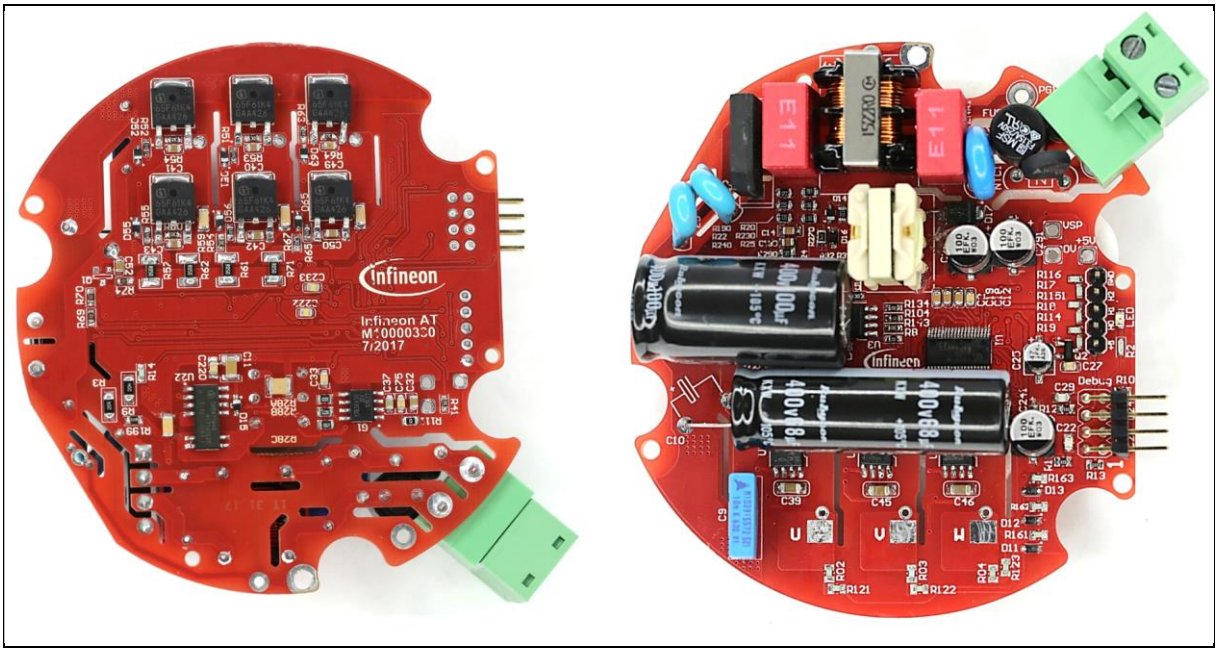
2.3 Benefits

- High efficiency
- Cost-effective
- Simplified design
- Accelerated time-to-market

2.4 Target applications

- Fans
- Fridges
- Pumps

3 Main features



The EVAL_100W_DRIVE_CFD2 is a complete evaluation board for motor drive application. The kit demonstrates Infineon's discrete power SJ MOSFET CoolMOS™ CFD technology for motor drives.

Main features:

- Maximum input voltage: 265 V AC or 370 V DC
- Minimum input voltage: 85 V AC or 120 V DC
- Output power for applied motor: up to 100 W without heatsink
- On-board EMI filter
- Current sensing for each phase configured by default
- Sensing of DC-link voltage
- +12 V auxiliary power supply based on QR Flyback
- Compact design using 650 V CoolMOS™ CFD, op-amp for current sensing and comparator
- On-board demodulator for speed and on/off control using potentiometer
- High efficiency and cost-effective
- Hardware and software over current (OC) protection
- Overvoltage (OV) and undervoltage (UV) detection
- Based on 32-bit ARM® Cortex™-M0 core-based microcontroller
- Firmware based on XMC1000 sensorless FOC motor control library
- Fully customized for fridge compressor, air-conditioning outdoor fan and ceiling fan applications
- FOC sensorless algorithm
- PCB size customized for cooling fan design
- PCB diameter: 87 mm

3.1 Key data

CoolMOS™ CFD2 is Infineon's latest series with an integrated fast body diode. It is the ideal choice for motor drive applications such as in home appliances markets, in which there is a need for high efficiency, while not compromising on high reliability and ease-of-use.

The fast reverse-recovery of CoolMOS™ CFD2 offers designers the benefits of reduced stress on the device while the body diode is not fully recovered, and an extra safety margin for repetitive hard-commutation in designs, which translates to reduced design-in effort.

- First 650 V technology with integrated fast body diode on the market
- Low switching losses due to low Q_{rr} at repetitive commutation on the body diode
- Self-limiting di/dt and dv/dt
- Low Q_{oss}
- Reduced turn-on/turn-off delay times
- Outstanding CoolMOS™ quality

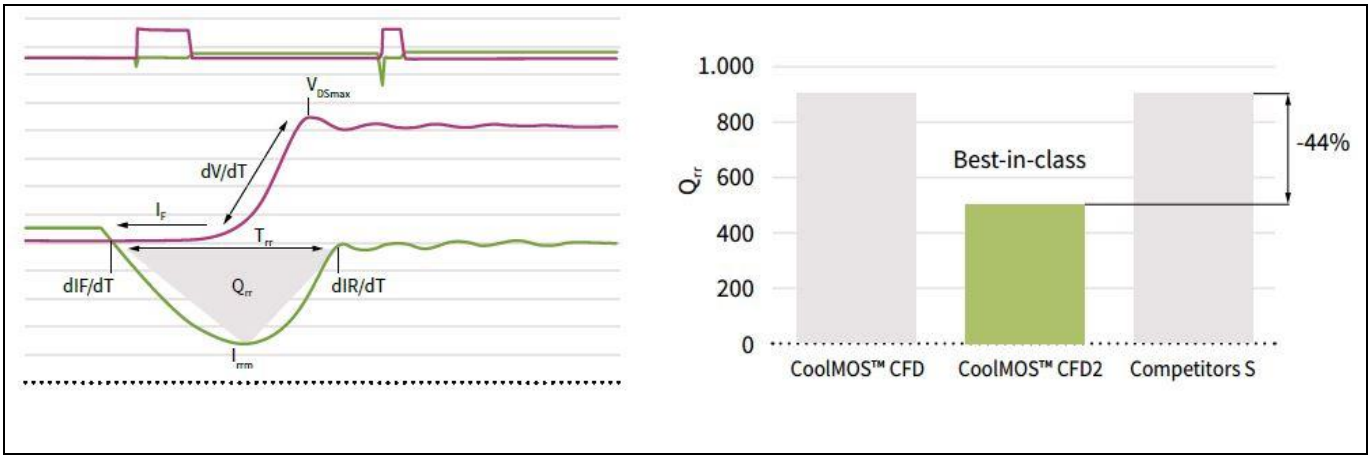


Figure 1 Highest reliability from lowest reverse-recovery charge and reverse-recovery time

For further information regarding CoolMOS™ CFD, such as static and dynamic electrical behavior, as well as thermal and mechanical characteristics, please refer to the datasheet of the IPD65R1K4CFD. Table 2 provides the absolute maximum ratings of the IPD65R1K4CFD.

Table 2 Absolute maximum ratings of CoolMOS™ IKD65R1K4CFD

Symbol	Description	Min.	Max.	Unit
V_{DSS}	MOSFET blocking voltage	–	650	V
IO @ T = 25°C	DC output current per MOSFET	–	2.8	A
Pd @ TC = 25°C	Maximum power dissipation per MOSFET	–	28.4	W
TJ	Operating junction temperature	-55	150	°C
TC	Operating case temperature	-55	150	°C
TS	Storage temperature	-55	150	°C
VSD	Diode forward voltage	0.9		V
t_{rr}	Reverse-recovery time	50		ns
Q_{rr}	Reverse-recovery charge	0.1		µC

3.1.1 Comparing SJ MOSFET vs IGBT

In conduction mode, the unipolar MOSFET acts like a resistor. In contrast, a bipolar IGBT device behaves like a resistor in series with a diode. Figure 2 illustrates similar conduction losses for MOSFET and IGBT modules. However, as the load current is reduced, the IGBT voltage remains relatively constant and the MOSFET voltage reduces linearly based on its R_{dsON}. In motor drive applications where the switching frequency is around 20 KHz, the conduction losses are the dominant losses in the application, especially at partial load points where the R_{dsON} of the MOSFET playes the key role of improving light-load efficiency.

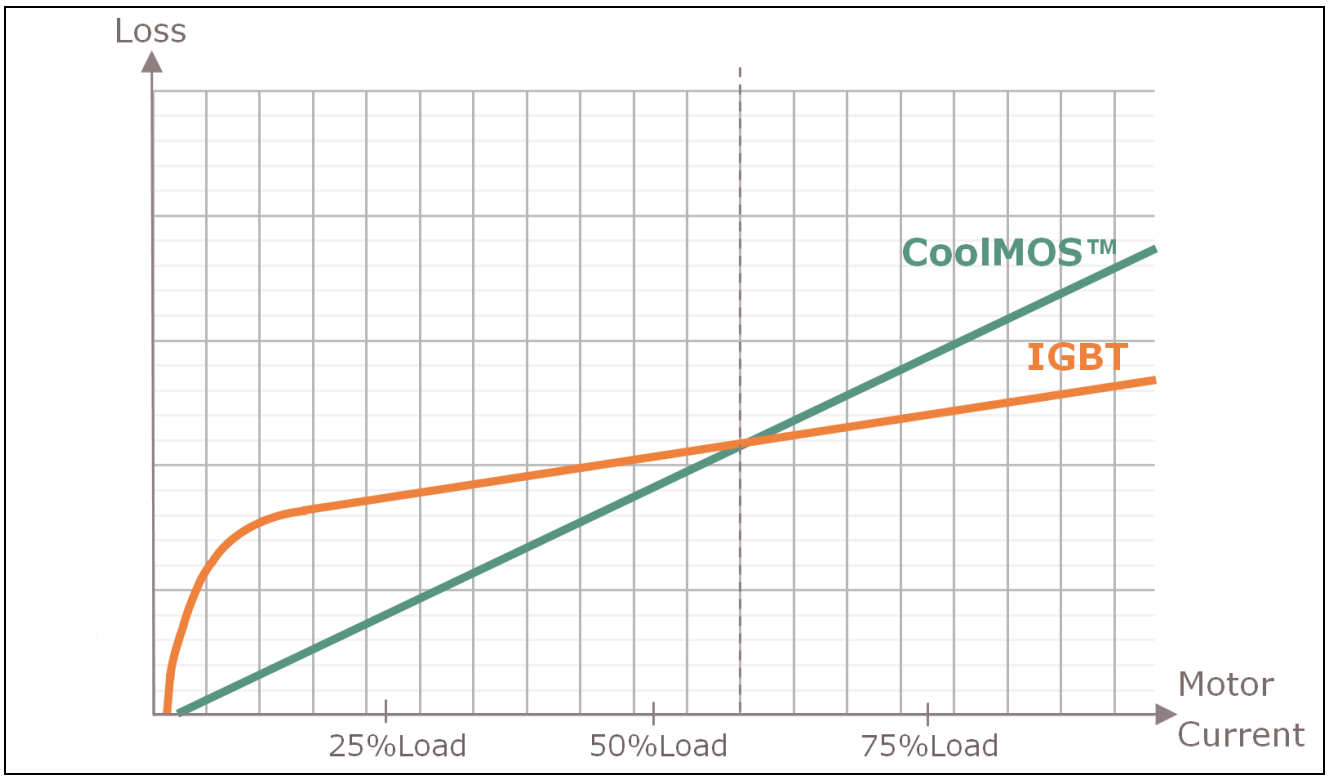


Figure 2 Conduction loss comparison (at the same current rating)

3.2 Specifications of the evaluation board EVAL_100W_DRIVE_CFD2

Table 3 shows the important specifications of the evaluation board EVAL_100W_DRIVE_CFD2.

Table 3 EVAL_100W_DRIVE_CFD2 board specifications

Parameters	Value	Conditions
Input		
Voltage	85–264 V_{rms}	
Frequency	50/60 Hz	
Input current	1.5 A_{rms}	
Output		
Power (three phases)	100 W	
Current per leg	500 mA	

Main features

Parameters	Value	Conditions
DC bus		
Maximum DC bus voltage	370 V	
Minimum DC bus voltage	120 V	
Current FB		
Phase Current sensing devices R61, R62, R71	0.05 Ω	The default configuration uses three shunts sensing in the emitter paths – IU+, IV+, IW+
overallCurrent protection devices R57	0.25 Ω	
Protections		
Output current trip level	2.4 A	Configured by either changing shunt resistors or adapting comparator threshold
On-board power supply		
12 V	12 V±5 %, max. 250 mA	Used for inverter gate driver power
5 V	5 V±5 %, max. 50 mA	Used for microcontroller supply and current sensing and over current protection circuit.

3.2.1 Functional groups

Figure 3 and Figure 4 show the functional groups of the EVAL_100W_DRIVE_CFD2 evaluation board.

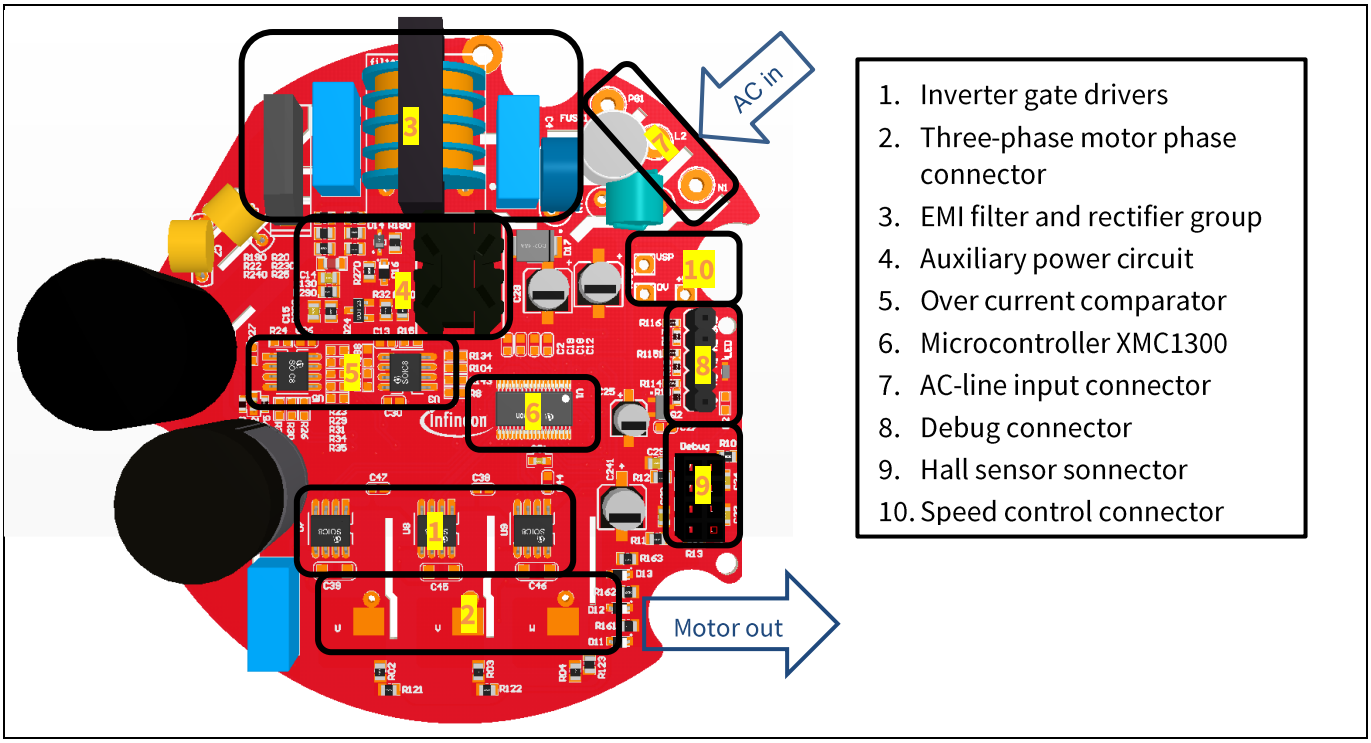


Figure 3 Functional groups of the EVAL_100W_DRIVE_CFD2 evaluation board's top side

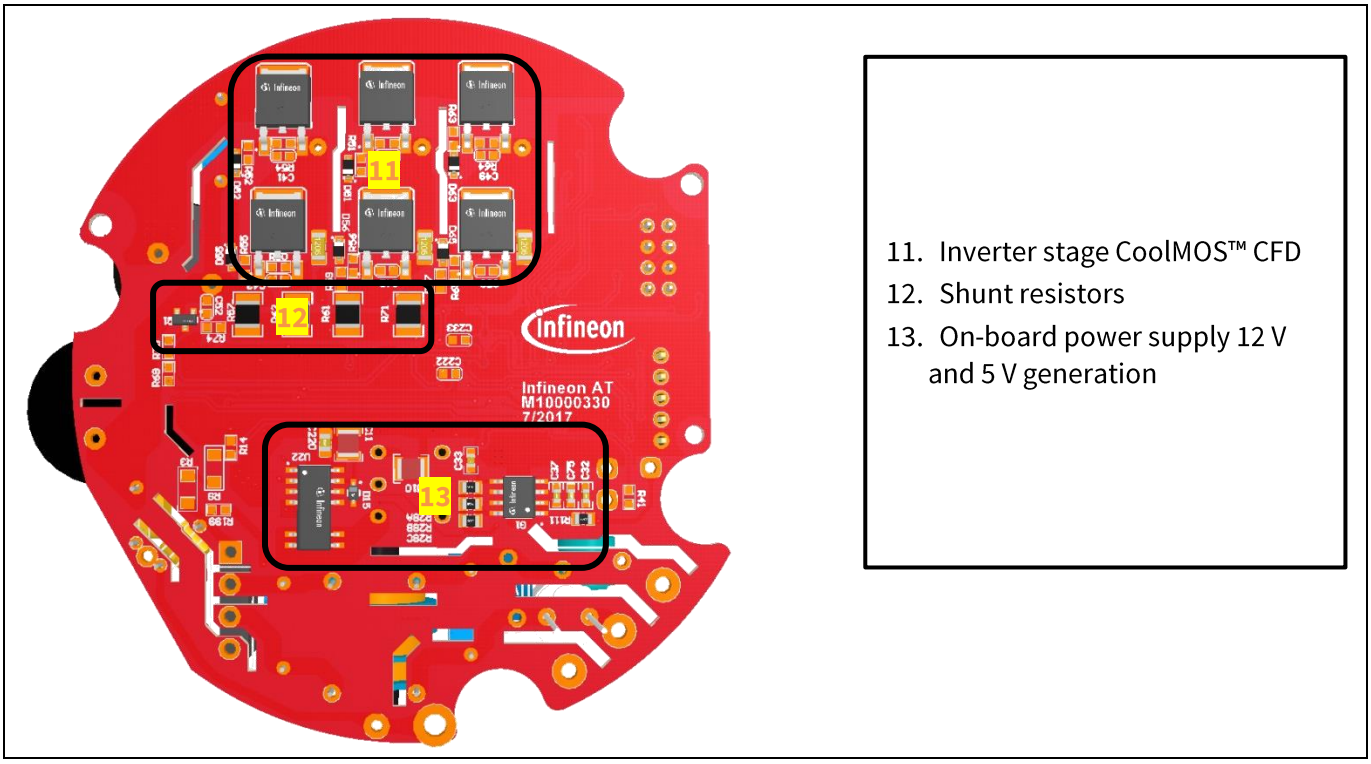


Figure 4 Functional groups of the EVAL_100W_DRIVE_CFD2 evaluation board's bottom side

4 Pin assignments

4.1 AC-line connector

This section gives general information on the connectors in the EVAL_100W_DRIVE_CFD2 evaluation board. Figure 5 includes the details of the line connector. It is possible to connect DC voltage to the AC connector, and in this case a permanent DC current will be conducted through the rectifier bridge. Maximum ratings are valid for AC as well as DC conditions. It is recommended to observe the temperature of the rectifier bridge. Due to this rectifier, the DC supply's polarity at the connector is of no concern. The evaluation board is protected by an on-board fuse rated 3 A.

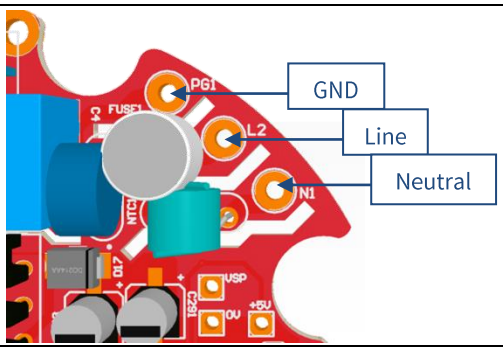


Figure 5 Line connector

4.2 Motor side connector

Figure 6 shows details of the three-phase motor side connection.

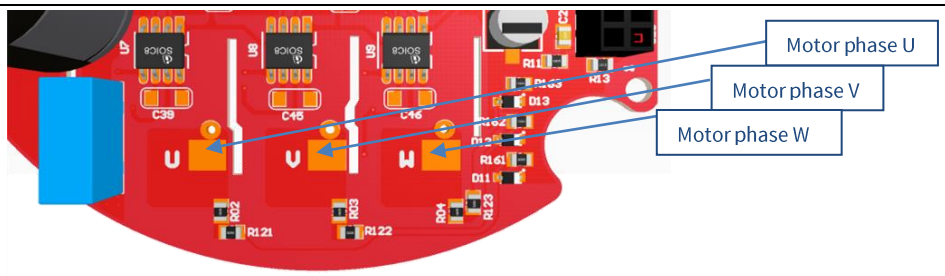


Figure 6 Motor side connector

4.3 Speed control potentiometer

Figure 7 shows details of the motor speed control potentiometer connection.

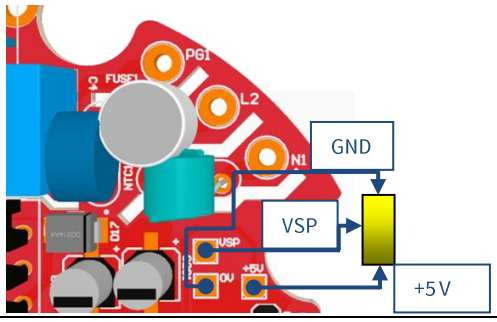


Figure 7 Speed control potentiometer connector

4.4 Eight-pin debug connector

The EVAL_100W_DRIVE_CFD2 supports debugging via serial wire debug (SWD) and serial port debug (SPD). Figure 8 shows details of pin assignment.

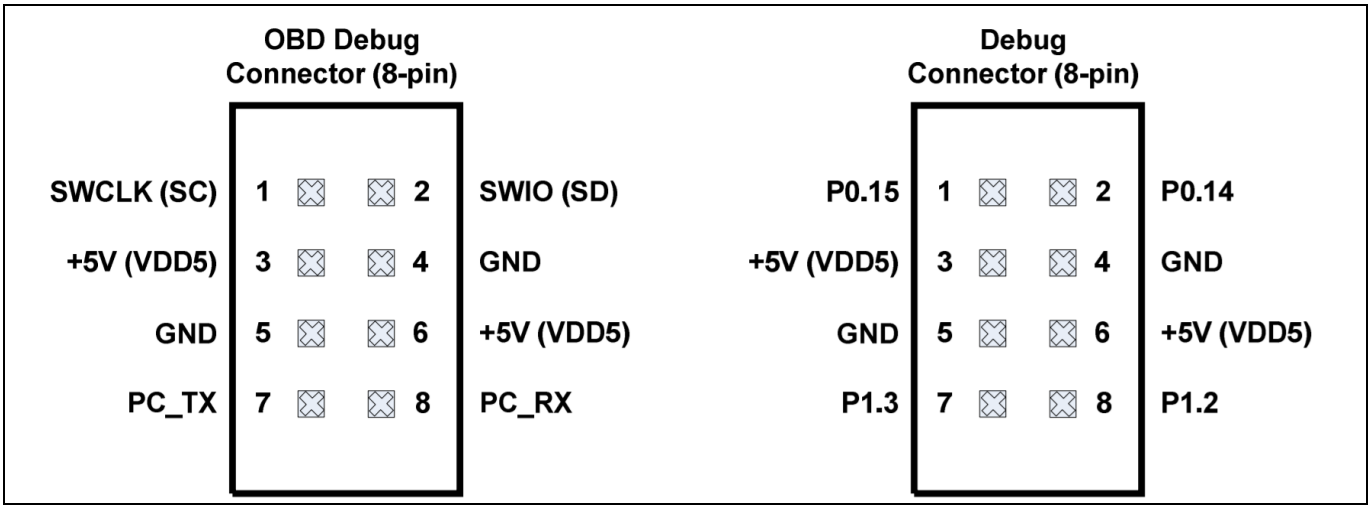


Figure 8 Pin assignment of the eight-pin debug connector

The default debug connections used in the EVAL_100W_DRIVE_CFD2 are as follows:

- SWD:
  - SWIO/SPD – P0.14 (SWD0)
  - SWCLK – P0.15 (SWD0)
- Full duplex UART communication via a virtual COM port:
  - PC_RXD – P1.2 USIC0CH1.DOUT0
  - PC_TXD – P1.3 USIC0CH1.DX0A

4.5 Hall sensor connector

The EVAL_100W_DRIVE_CFD2 provides hall connectors as indicated in Figure 9. The hall sensor interface provides a pull-up resistor for each hall sensor signal as well as +5 V power supply for the hall sensors.

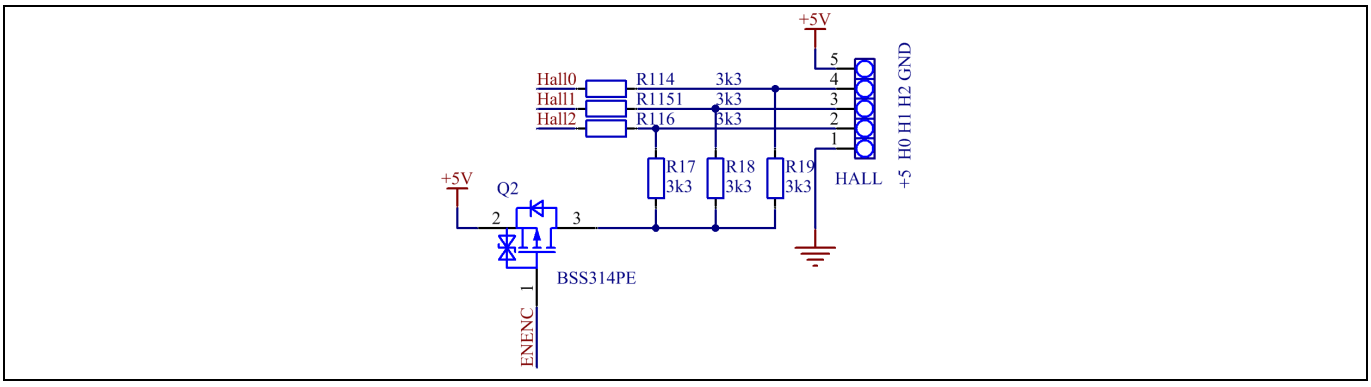


Figure 9 Hall sensor connector

5 Schematics and layout

To meet individual customer requirements and make the EVAL_100W_DRIVE_CFD2 evaluation board a basis for development or modification, all necessary technical data such as schematics, layout and components are included in this chapter.

5.1 EMI input filter and rectifier circuit

Figure 10 depicts the schematic from the AC-line input connector to the rectified DC bus voltage. This circuitry includes a passive EMI filter consisting of elements C4, C5, filter1, C3 and C7, a 2 A/600 V rectifier block U2, and an NTC inrush current-limiting NTC 1 for surge current protection. Two electrolytic capacitors C10, C6 and ceramic capacitor C9 are used for buffering the rectified DC bus voltage DC+. The design is protected by a 3 A fuse FUSE1 on the line input terminal L1.

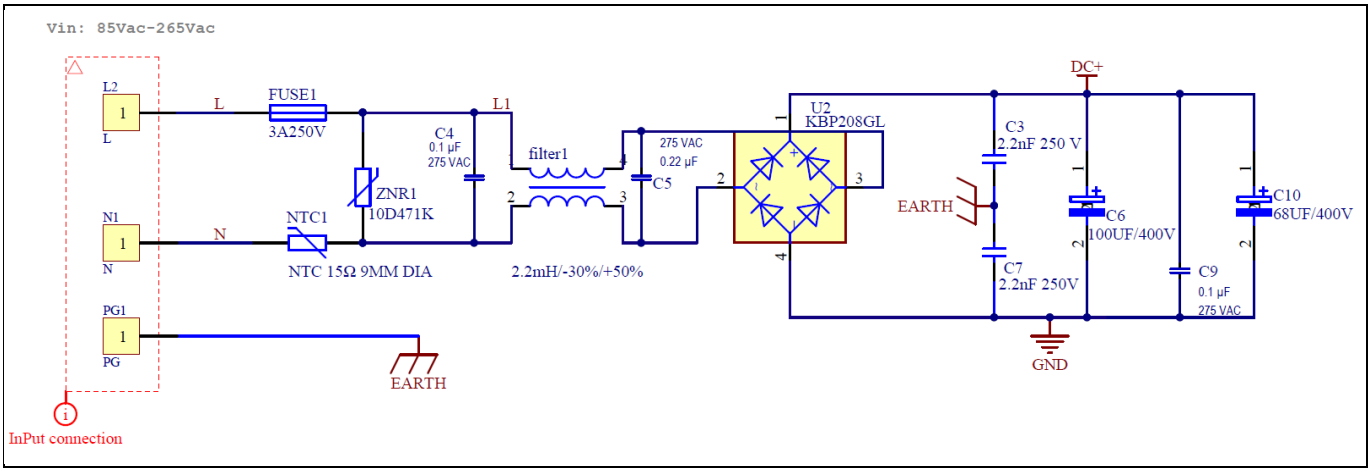


Figure 10 Schematic for EMI input filter and AC-DC section of the EVAL_100W_DRIVE_CFD2 evaluation board

5.2 Three-phase inverter using CoolMOS™ CFD

The three-phase power inverter is implemented using six CoolMOS™ CFDs (IPD65R1K4CFD). Each inverter leg has its own shunt in the low-side path for phase current measurement. In addition the common DC-link current can be measured by its own shunt.

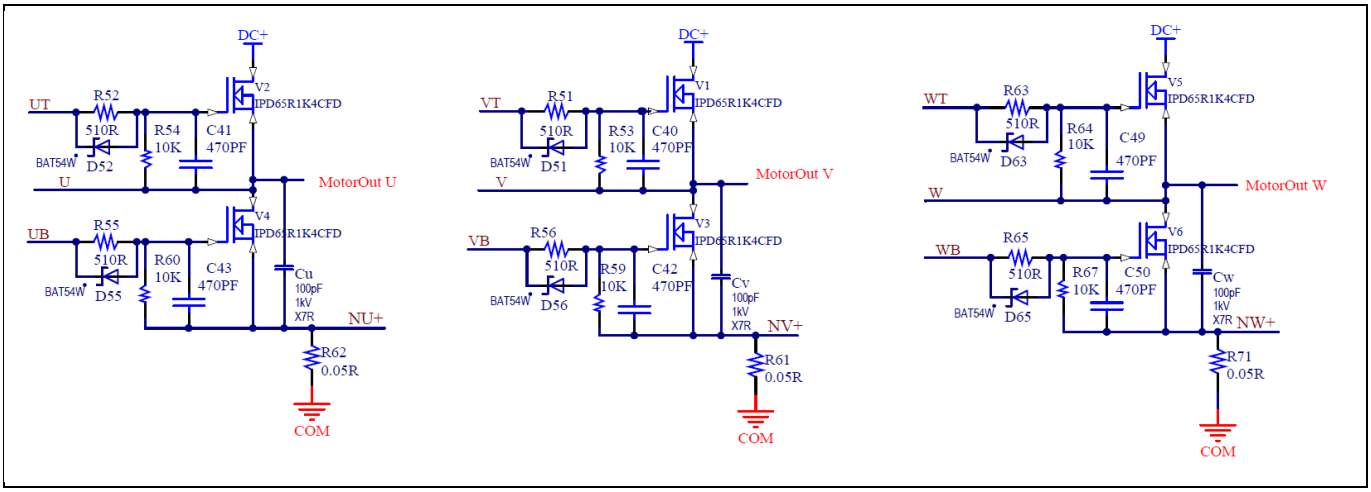


Figure 11 Schematic of the three-phase inverter on the EVAL_100W_DRIVE_CFD2 evaluation board

The inverter section is implemented as shown in Figure 11. The design includes the same gate circuit for the high-side and low-side MOSFETs. The R_{Gon} = 510 Ω is used to reduce turn-on dv/dt = 4.8 V/ns, leading to less HS V_{gs} spike 1.1 V, shorter plateau, and less turn-on loss, while R_{Goff} = 0 Ω is used for less impedance to GND at turn-off, which results in reduced voltage coupling spike, as shown in the waveforms in Figure 12.

Care must be taken when choosing R_{Gon}, because low R_{Gon} would result in faster turn-on, and in turn lead to high di/dt for the low-side body diode and high reverse-recovery. Using much higher R_{Gon} would isolate the gate circuit from the MOSFET, causing high-side V_{gs} spike, which if greater than V_{th} will cause a faulty turn-on of the MOSFET. More details are described in the "Slew rate control of CoolMOS™" section.

Adding C_{gs} = 0.47 nF reduces C_{rss}/C_{iss} ratio for less drain-gate (Miller) coupling gain.

Adding C_{ds} = 100 pF controls and linearizes the dv/dt at the switching node (see Figure 13), and this has the benefit of removing any gate oscillation, and improving EMI.

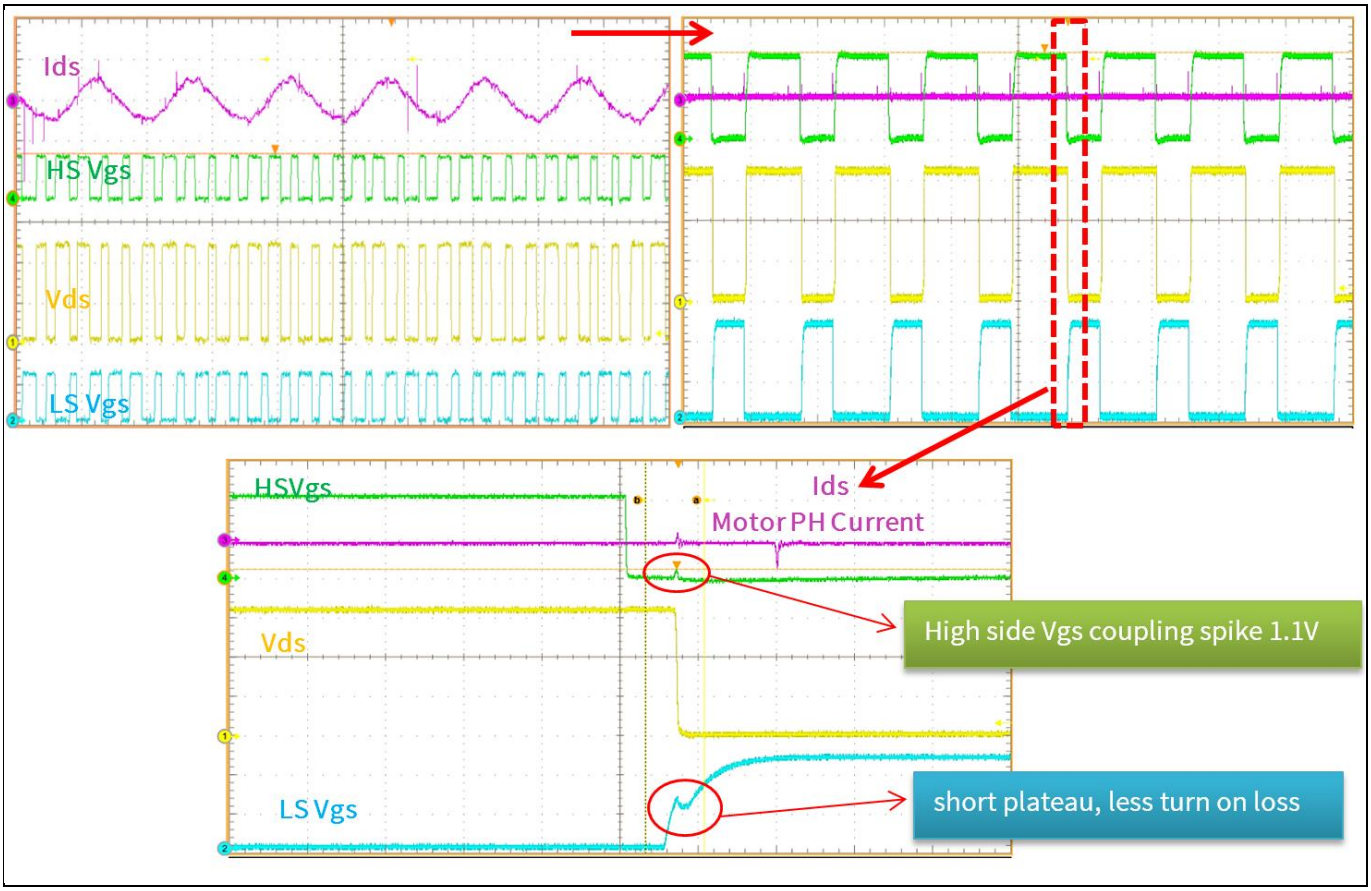


Figure 12 Motor Phase waveforms

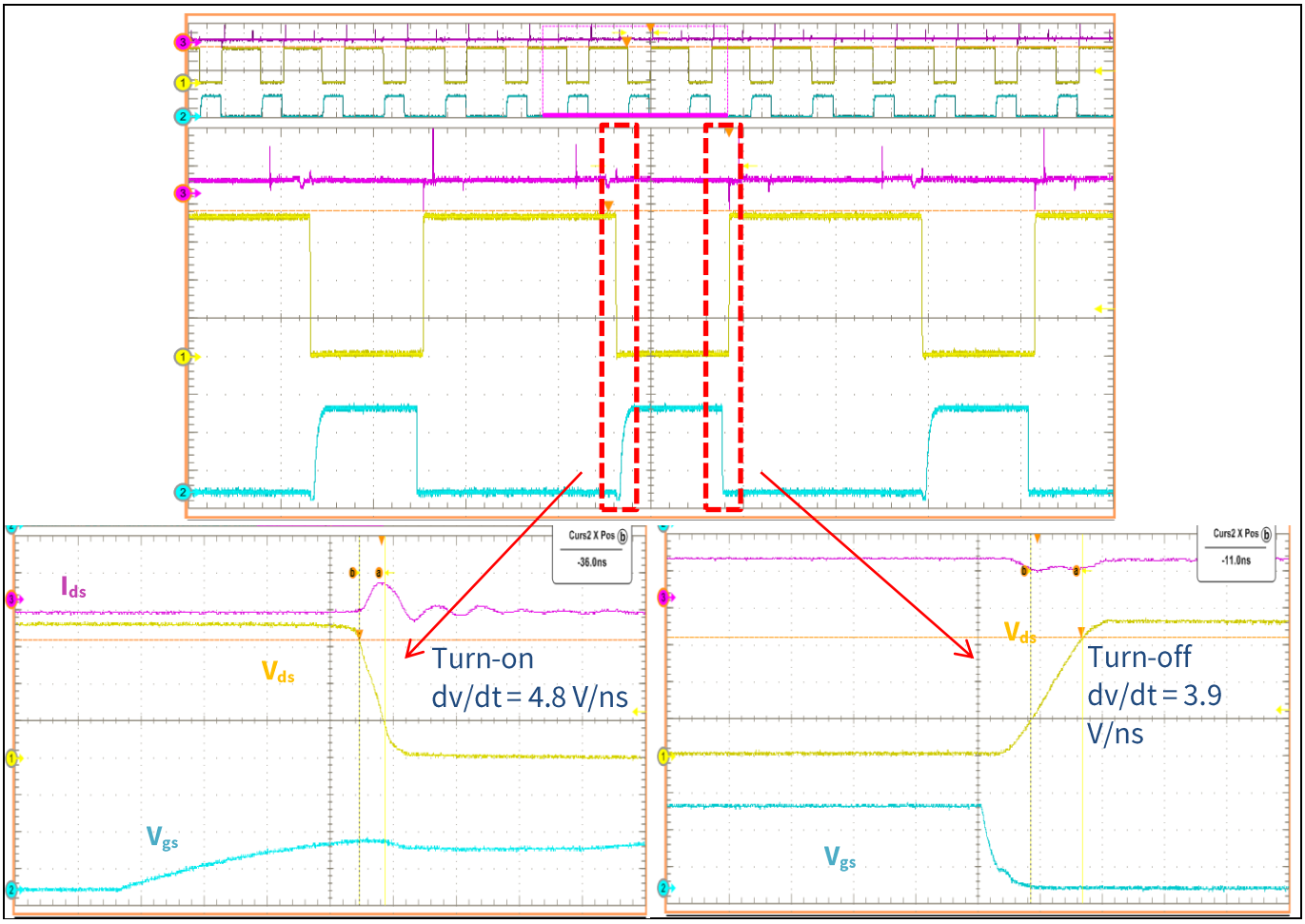


Figure 13 Controlled dv/dt

5.3 Power supply

Figure 14 depicts the schematic of the control power supply available on the EVAL_100W_DRIVE_CFD2 board. The bias supply using the CoolSET™ ICE5QR4770AG operates from an AC input voltage from 85 V_{AC} to 265 V_{AC} providing a non-isolated +12V output. The linear regulator (IFX1763XEJV50) generates +5 V from the +12 V provided by the flyback circuit. The +5 V power supply is used to supply the over current comparator circuit and the XMC microcontroller.

5.4 QR controller (CoolSET™)

The QR CoolSET™ series continues to deliver design agility and miniaturization. The CoolSET™ is an integrated power management IC with a 700 V avalanche rugged CoolMOS™, start-up cell, and QR current mode flyback PWM controller in a DSO-12 package. This new series offers the possibility of higher efficiency and better EMI performance. The digital frequency reduction feature ensures a very stable operation with decreasing load change and the fold-back correction keeps the maximum power limits within the tolerance desired by SMPS designers. The Active Burst Mode (ABM) operation during low power consumption provides best-in-class power consumption during standby.

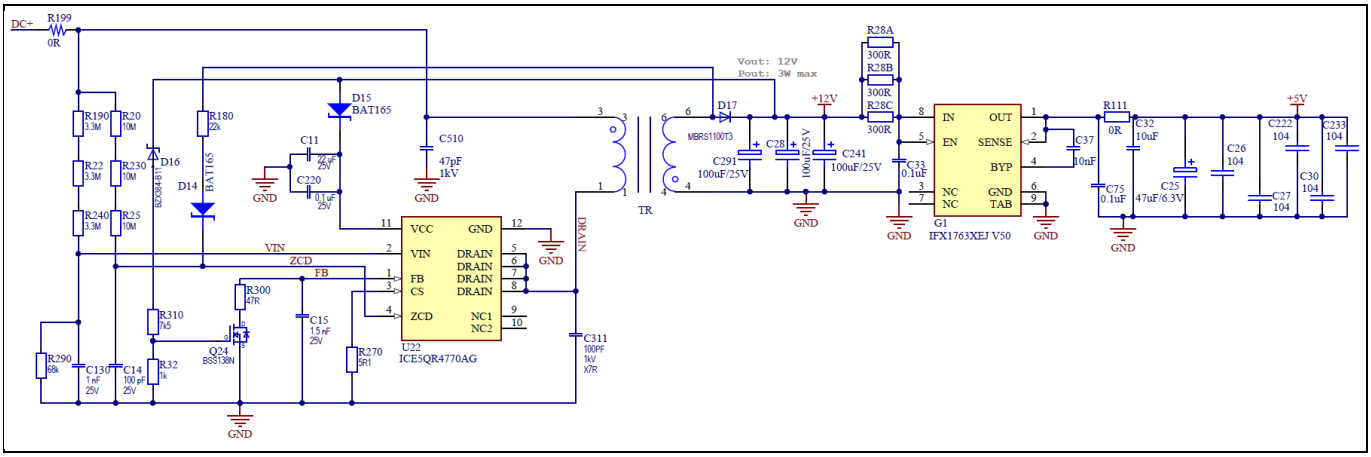


Figure 14 Power supply section of the EVAL_100W_DRIVE_CFD2 evaluation board

5.4.1 System benefits

The 3 Watt power supply that provides the +12 V and +5 V voltage rails is designed using a quasi-resonant flyback converter topology using the 5th generation quasi-resonant CoolSET™ (ICE5QR4770AG). With the CoolMOS™ integrated in this IC, it simplifies the design and layout of the PCB. The improved novel digital frequency reduction with proprietary quasi-resonant operation offers lower EMI and higher efficiency for a wide AC range by reducing the switching frequency difference between low and high line. The enhanced active burst mode power enables flexibility in standby power operation range selection and quasi-resonant operation during active burst mode. As a result, the system efficiency, over the entire load range is significantly improved compared to a conventional free running quasi-resonant converter implemented with only maximum switching frequency limitation at light load. In addition, numerous adjustable protection functions have been implemented in ICE5QR4770AG to protect the system and customize the IC for the chosen application. The CoolSET™ controller also has protectionsn case of failure modes such as, brownout or line over voltage, V_{CC} over/under voltage, open control-loop or over load, output overvoltage, over temperature, V_{CC} short to ground, and CS short to ground. Under any of these conditions the device enters into a protection mode. By means of the cycle-by-cycle peak current limitation, the dimension of the transformer and current rating of the secondary diode can both be optimized. Thus, a cost effective solution can be easily achieved.

The efficiency improvement of the new CoolSET™ (ICE5QR4770AG) design can be seen in Figure15. The efficiency improvement is between 10.4% and 25% over the 1W to 6W load range, compared to the old generation of CoolSET™ (ICE3RBR4765JG).

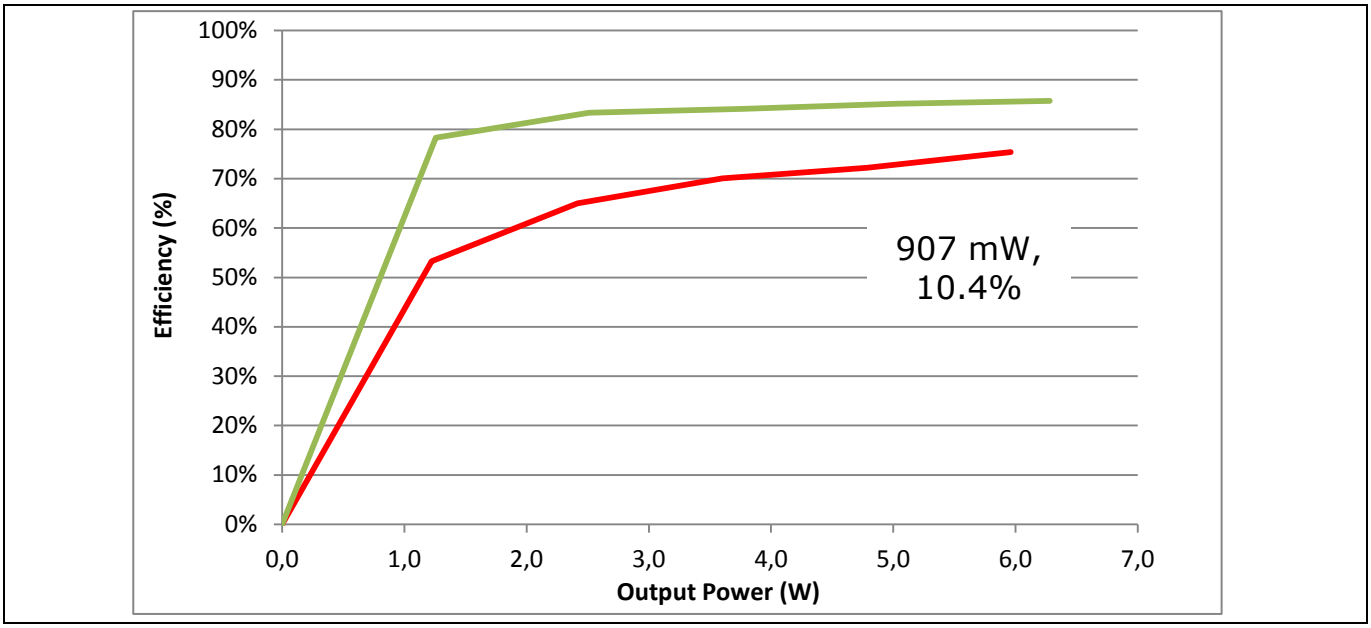


Figure 15 Efficiency comparison new CoolSET™ (ICE5QR4770AG) vs. old CoolSET™(ICE3RBR4765JG)

5.4.2 CoolMOS™ C3 to P7 benefits

The old generation of CoolSET™ used the C3 CoolMOS™ technology. By switching to the latest P7 CoolMOS™ technology the benefits of the latest technology can be gained. The gate driving losses of the device are lower and the $R_{DS(on)}$ change vs. temperature is lower than the previous generation of devices. The P7 also has lower output capacitance energy storage vs. voltage, but in this design some of these benefits are reduced by the additional C_{DS} capacitor that needs to be added for the snubberless operation as stated below.

5.4.3 Quasi resonant flyback controller

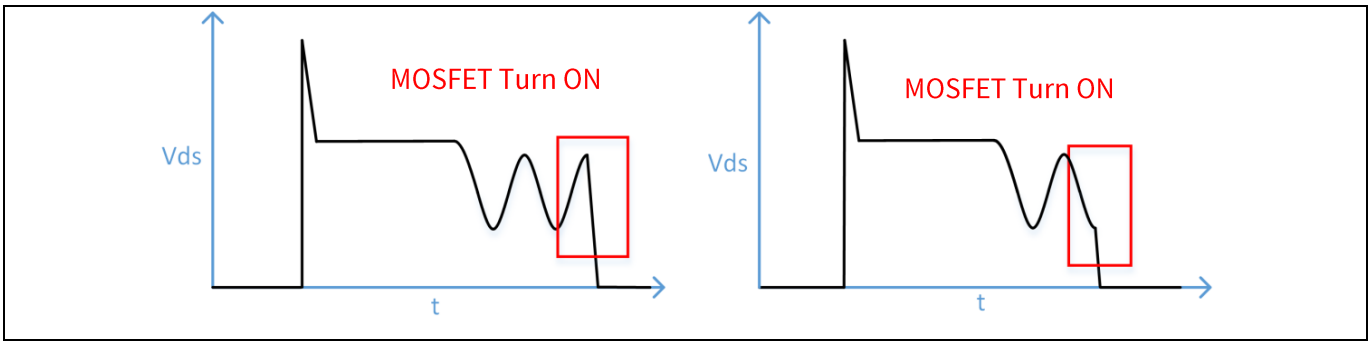


Figure 16 Fixed frequency flyback primary MOSFET drain source waveform (left) vs. a QR flyback primary MOSFET drain source waveform (right).

The QR Flyback helps to reduce the switching losses in the MOSFET by using the DCM resonant period of the flyback and then only turning on the MOSFET in this valley.

Since the turn-on switching losses are a function of V^2 (as shown below), this reduces the overall system switching losses. This has the added benefit of lowering the amount of switched energy which helps reduce switching noise from the converter, resulting in lower radiated and conducted emissions.

$$P_{sw_on} = 0.5 f_{sw} C_{OSS} V_{DS}^2$$

5.4.4 Snubber less design

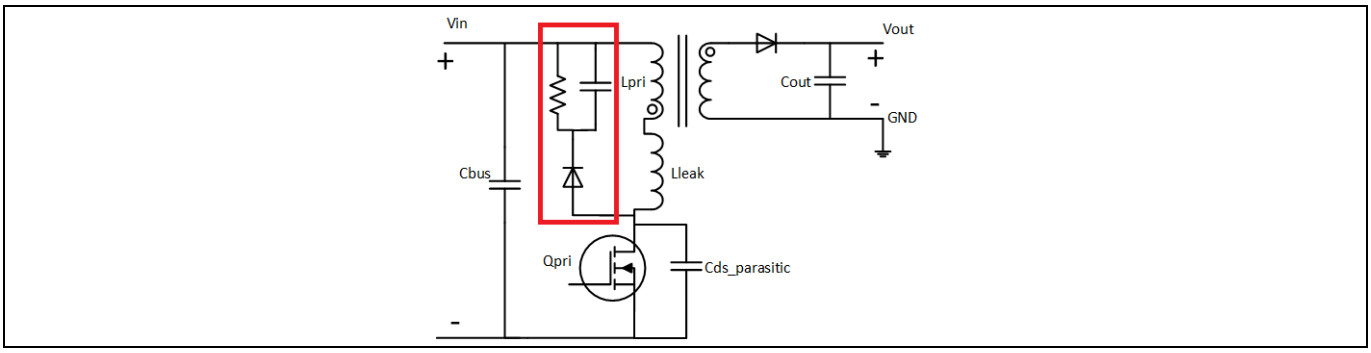


Figure 17 Snubber Network

The RCD snubber network dissipates energy every switching cycle regardless of the load since the RCD capacitor is charged up to the reflected voltage of the secondary. By removing the snubber network and switching to a snubberless design the overall efficiency was improved. This requires an additional 100 pF capacitor on the drain source of the MOSFET in order to provide energy storage for the leakage energy at full load. This still ends up in a net efficiency improvement over the RCD snubber network and takes up less board area and reduces the design cost. 10% margin was kept from the drain source breakdown voltage to the peak drain source voltage seen on the MOSFET during full load and maximum DC input voltage operation.

5.5 Current sense and over current protection circuit

Figure 18 shows the motor phase 5.5 Current sense and over current protection circuitry. The design offers hardware and software current detection, and the average current flow through the DC-link shunt resistor R57 is sampled every cycle of PWM. This value is read to detect over current. Once this condition occurs, the reference motor speed is scaled down by a factor until the current is within the limit defined in the user configuration file. Moreover, the three-phase motor currents are sensed separately though the differential operation amplifiers and sent back to the microcontroller through IU, IV and IW. In addition the overall current of the motor is sensed throw the DC-link shunt resistor R57, which activates the switch Q1 that in return sends a FAULT signal to the microcontroller to interrupt the PWM modulation and immediately stop all output to the motor.

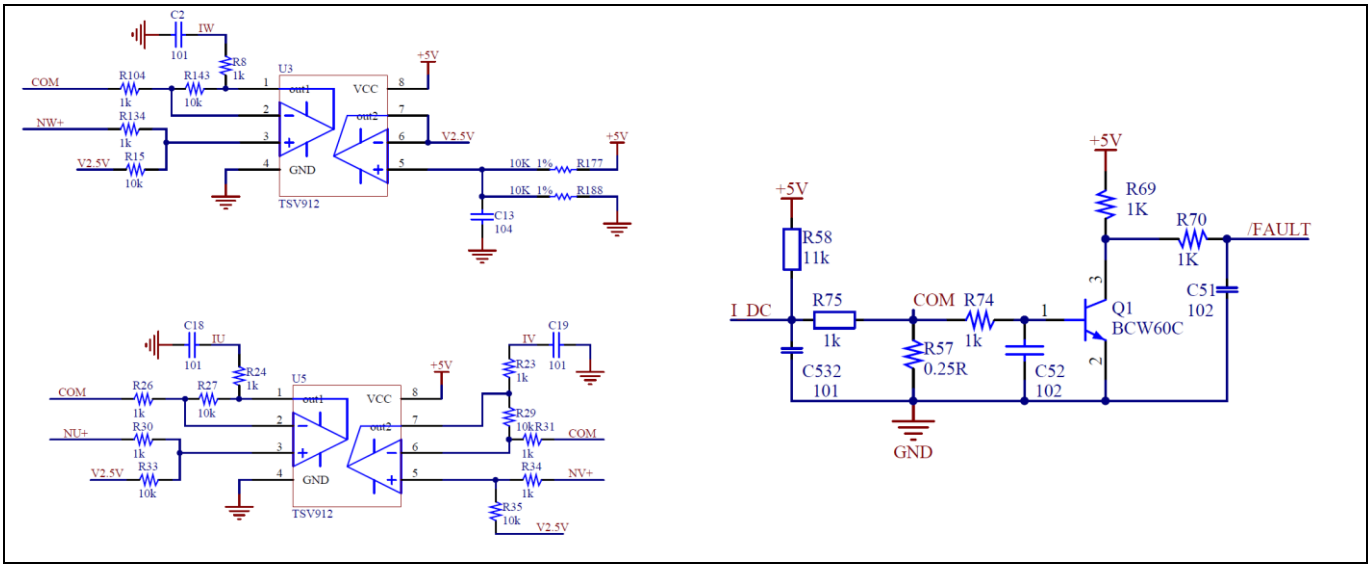


Figure 18 Over current circuit

The EVAL_100W_DRIVE_CFD2 provides an operational amplifier which amplifies the voltage drop over the shunt per phase with a gain of 10 (see waveforms in Figure 19). The amplified voltage information is sent back to the microcontroller through IU, IV and IW. The amplified voltage is calculated with $V = I_{shunt} \times R_{shunt} \times 10$.

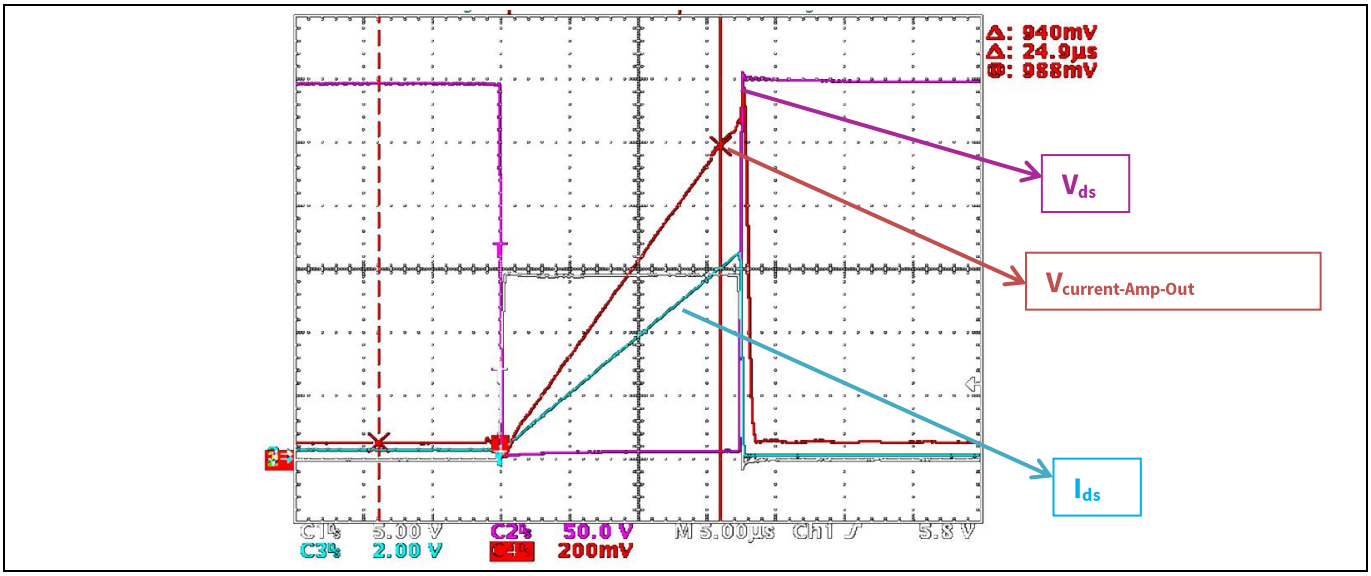


Figure 19 Current amplifier output and corresponding drain current

5.6 DC-link voltage measurement

Pin 2.4 of the microcontroller provides access to the DC-link voltage. Figure 20 provides the DC bus sense resistor details.

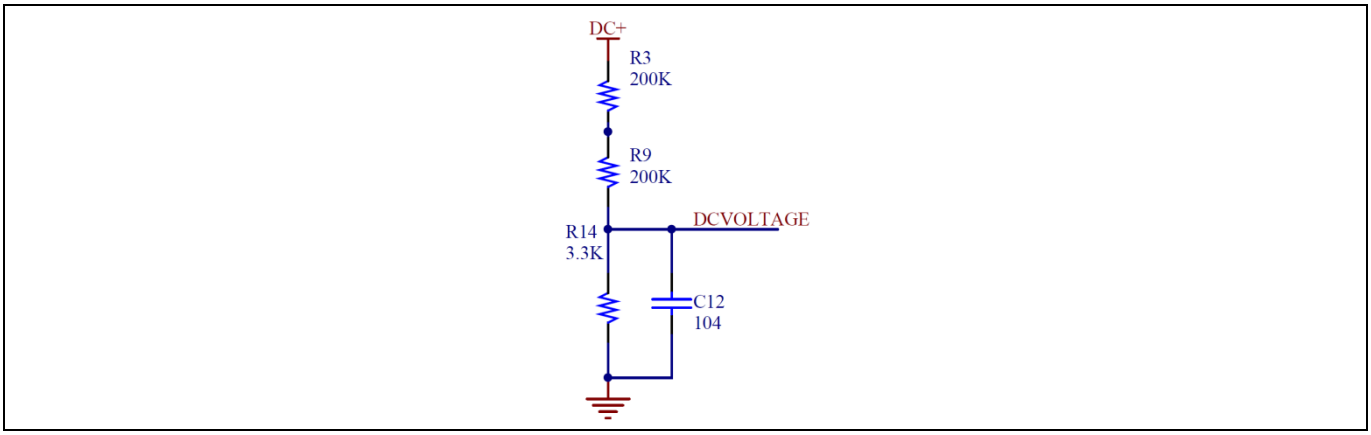


Figure 20 The DC bus sense resistor on the EVAL_100W_DRIVE_CFD2 evaluation board

The $DC_{VOLTAGE}$ provides input to the microcontroller with a voltage range of 0 V to 3.3 V on pin 2.4, reflecting a DC bus voltage range of 0 V to 400 V. If no feedback is desired from the $DC_{VOLTAGE\text{-}pin}$, R3 or R9 should be removed to avoid HV on the connector.

5.7 Output voltage (B_{EMF}) signal dividers

The power inverter outputs can be monitored at signals B_{EMF_U}, B_{EMF_V} and B_{EMF_W} with a ratio of 611 V : 5 V. See Figure 21 for details.

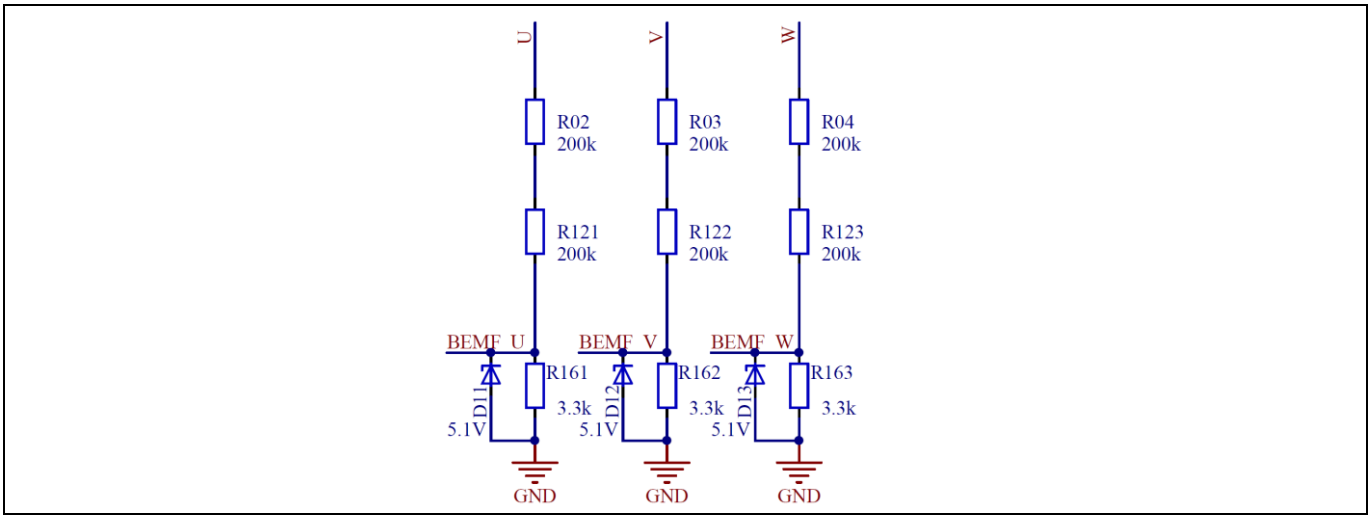


Figure 21 Output voltage (B_{EMF}) signal dividers

5.8 EiceDRIVER™ 2EDL non-isolated gate driver for MOSFETs

5.8.1 Introduction

The 2EDL family contains devices that control power devices with a maximum blocking voltage of +600 V in half-bridge configurations. Based on the existing SOI-technology, they provide ruggedness with transient voltages. No parasitic thyristor structures are present in the device, which means no parasitic latch-up can occur, at all temperature and voltage conditions.

The device includes a UV detection unit with hysteresis characteristics that are optimized either for IGBT or MOSFET. It support UV lock-out levels, and has an integrated ultrafast bootstrap diode. Additionally, the off-line gate-clamping function provides inherent protection for the transistors against parasitic turn-on by floating gate conditions, when the IC is not supplied via VDD.

5.8.2 Main features

- Thin-film SOI-technology
- Maximum blocking voltage +600 V
- Individual control circuits for both outputs
- Filtered detection of UV supply
- All inputs clamped by diodes
- Active shut-down function
- Asymmetric UV lock-out thresholds for high-side and low-side
- Qualified according to JEDEC1 (high-temperature stress tests for 1000 h) for target applications

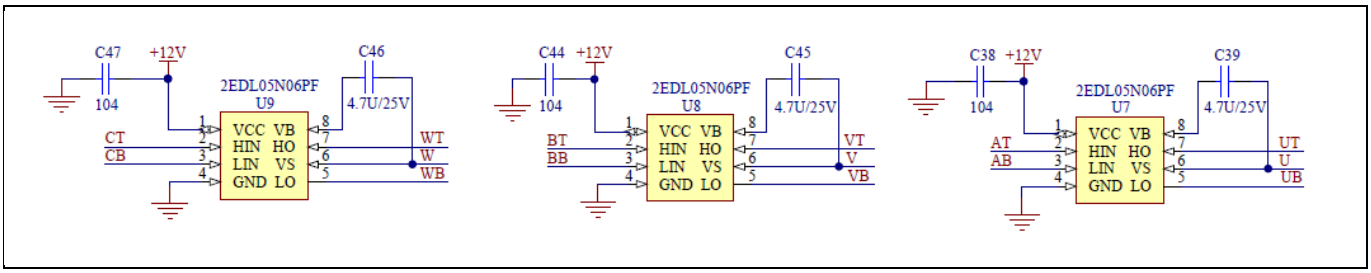


Figure 22 Power inverter – gate driver

The +12 V supply V_{CC} is monitored by the 2EDL05N06PF. In case of a UV the driver output is switched off. The thresholds for the low-side are typically VCCUV+ = 9.1 V (positive going) and VCCUV– = 8.3 V (negative going). The thresholds for the high-side are typically VBSUV+ = 9.1 V (positive going) and VBSUV– = 8.3V (negative going).

The three capacitors C39, C45 and C46 are used as bootstrap capacitors to provide the necessary floating supply voltages VB1, VB2 and VB3 respectively.

6 Slew rate control of CoolMOS™

High switching rates of MOSFET drain-source voltage during PWM operation in motor drive inverters cause displacement currents over the parasitic capacitance of the motor to the protected earth. These currents flow dominantly through the bearings, which leads to an accelerated aging of the bearings. This is a well-known failure mechanism and can be explained by the function of the switching frequency of the inverter as well as of the switching speed of the inverter's MOSFET.

The fewer switching instances, the less current is being measured. The same effect can be seen with the slower ramping of the drain-source voltage of the MOSFET. The slower the turn-on and turn-off, the less current flows through the bearings, and so switching slowly is always correlated with increased switching losses. The aim is to tune the switching processes toward low switching speed for all applications where high availability or little maintenance is desirable.

6.1 Reducing MOSFET dv/dt

A typical MOSFET turn-on and turn-off has been analyzed in many papers. A MOSFET can be modelled as shown in Figure 23.

Our area of interest is the dv/dt feature of the MOSFET and the parasitics that impact this.

$$dv/dt = V_{Gsth} / (R_G * C_{GD})$$

Hence, the lower the R_g and C_{gd}, the higher the dv/dt.

$$C_{OSS} = C_{GD} + C_{DS}$$

And, the lower the C_{oss}, the higher the dv/dt.

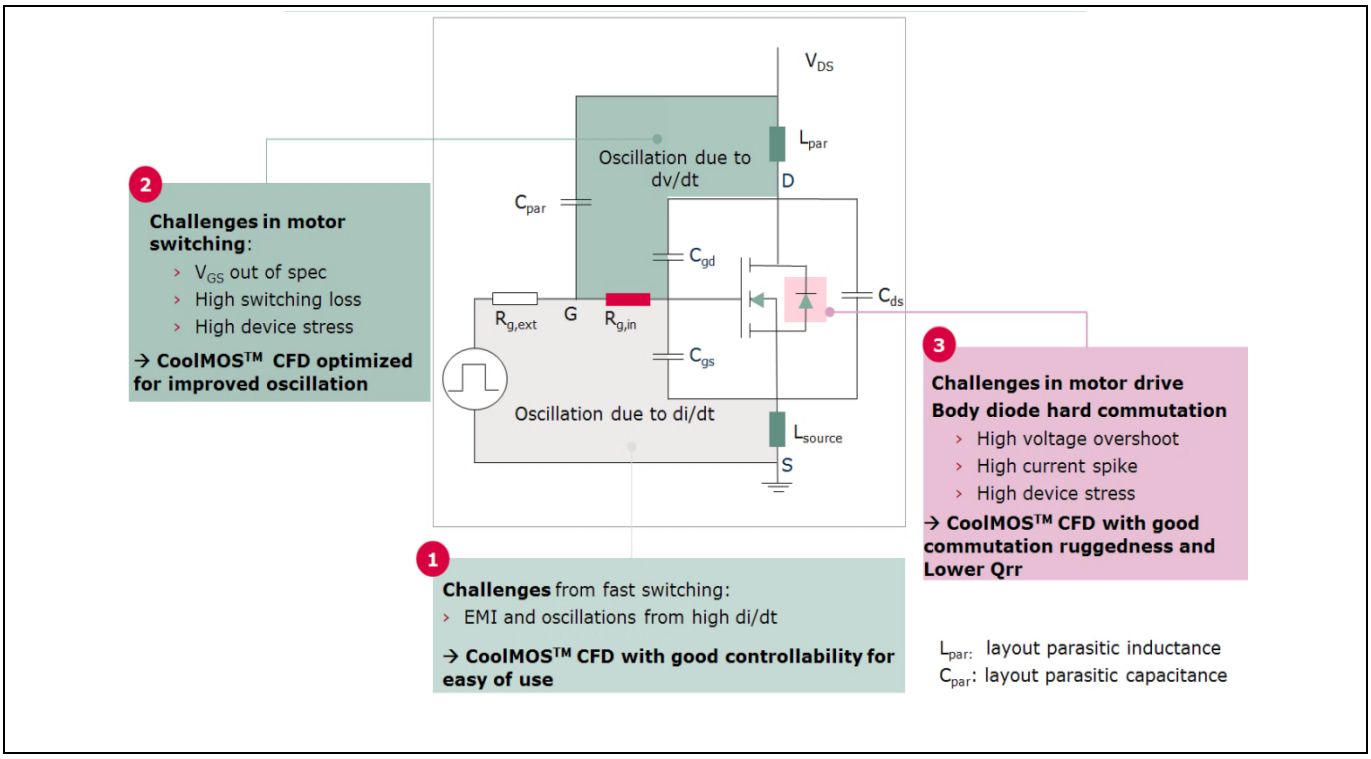


Figure 23 Design challenges and value offered by CoolMOS™

The above shows that we can clearly see the four parameters that can be modified to reduce dv/dt. They are:

- Increasing drain-source capacitor C_{DS}
- Increasing external gate resistor R_G
- Increasing gate-source capacitor C_{GS}

Higher C_{DS} reduces the dv/dt and reduces the V_{DS} overshoot.

Higher C_{GD} essentially increases the duration that the MOSFET stays in the Miller plateau and so slows the dv/dt. This leads to increased switching losses, thereby reducing the efficiency and increasing the temperature of the MOSFET.

Standard MOSFETs have a large C_{DS} and hence a slower dv/dt. The large C_{DS} also helps in meeting the radiated EMI. Therefore, if a small resonant capacitor (C_{DS}) is used in consideration of the radiated noise, high efficiency can be achieved. Hence there is a trade-off between meeting the radiated EMI requirement and meeting efficiency targets.

Whenever the internal parasitics (C_{GD} and C_{DS}) of the MOSFET are low, it may become necessary to use an external capacitor C_{DS} to ensure a reduced dv/dt. The external capacitors are in the range of 10 pF to 100 pF and give the designer a fixed value with which to design for these parasitic capacitances. Standard MOSFETs have larger internal capacitances, as seen in their datasheets. Hence, when they are replaced by CoolMOS™, external C_{DS} is needed to slow the fast-switching SJ MOSFET and control/linearize dv/dt at turn-on, and this has the benefit of removing any gate oscillation and reducing EMI.

An external C_{GS} capacitor can also be added at the gate, and this option helps to slow down the dv/dt, damp down the di/dt of the switching MOSFET and reduce the C_{rss}/C_{iss} ratio, which helps to avoid any unwanted return-on due to the Miller effect.

As described in section 6.3 of this AN, “Avoiding parasitic switching”, it is preferable to have a different set of R_G values in the turn-on and turn-off conditions of the MOSFET. A lower value of R_{Goff} is required, to reduce switch-off losses and lower voltage coupling spikes by ensuring good coupling to ground. To reduce turn-on voltage spikes and dv/dt, a higher value of R_{Gon} is required.

The internal R_G inside the MOSFET is needed to ensure smooth turn-on and turn-off behavior by internally damping the oscillations due to poor PCB layout. CoolMOS™ CFD has an integrated R_G that must be considerd when selecting the external R_{Gon} and R_{Goff} (which should include the internal R_G values based on the R_{dsON} used).

A higher R_G value not only degrades the MOSFET’s working conditions by increasing the temperature and switching losses, but also degrades application efficiency and working conditions by fully modifying the switching behavior of the device. A higher R_G affects the driver/PWM controller heavily, requiring it to sustain a higher temperature, as well as dissipating more power to charge the MOSFET input capacitance. It also potentially produces cross-conduction that may cause system disruption due to static dv/dt. The techniques for reducing dv/dt are summarized in section 5.2, “Three-phase inverter using CoolMOS™ CFD”.

6.2 Turn-on via the Miller capacitance

When turning on the lower MOSFET in a half-bridge a voltage change dv_{DS}/dt occurs across the upper MOSFET/diode. This causes an approach current $i_{GD} = C_{GD} \times dv_{DS}/dt$ to flow, which charges the parasitic capacitance C_{GD} of the upper MOSFET. The capacitances C_{GD} and C_{GS} form a capacitive voltage divider. Figure 21 depicts the current path via the Miller capacitance of the upper MOSFET.

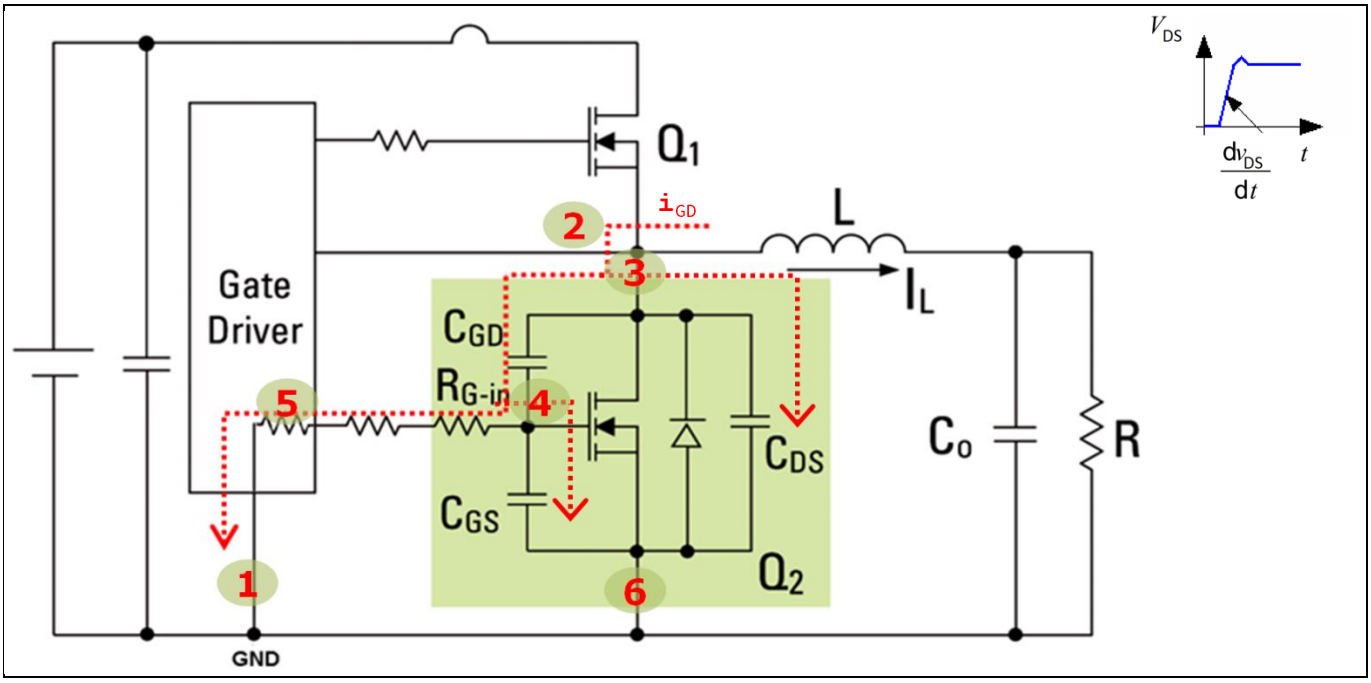


Figure 24 Current via the Miller capacitance

1. Driver connects gate to ground.
2. A constant current i_{GD} driven by the commutation cell flows to the drain terminal.
3. The current will be split into C_{gd} and C_{ds}.
4. Ideally the major part of the current will flow to the gate driver and the minor part to C_{gs}.
5. L_{stray} in the gate path avoids the current flow to the gate and larger current flows to C_{gs} and consequently the voltage on C_{gs} will rise and the channel is turned on.
6. Additionally, there is a voltage drop on L_{source}.

The current i_{GD} flows via the Miller capacitance, the serial resistors, C_{GS} and the DC bus. If the voltage drop across the gate resistor exceeds the threshold voltage of the MOSFET, a parasitic turn-on occurs. With a rising chip temperature the threshold voltage drops by several mV/K. When the upper MOSFET switches, a current flows via the Miller capacitance of the lower MOSFET and may lead to parasitic turn-on here as well.

Note: *Ratio* $(\boldsymbol{Qgs} + \boldsymbol{Qgd})/(\boldsymbol{Ciss}.\boldsymbol{Vth}) < \mathbf{1}$ *no return-on possible.*

Note: *Ratio* $(\boldsymbol{Qgs} + \boldsymbol{Qgd})/(\boldsymbol{Ciss}.\boldsymbol{Vth}) >= \mathbf{1}$ *return-on possible.*

Note: *Large L_{stray} value leads to more current into C_{gs} and a higher probability of return-on.*

Note: *Large R_g value leads to more current into C_{gs} and a higher probability of return-on and higher dependency device deviation and efficiency.*

6.3 Avoiding parasitic switching

6.3.1 Variation of the gate resistor

The voltage change dv_{DS}/dt and the current change di/dt during the turn-on process may be influenced by varying the gate resistor R_{Gon}. Increasing the gate resistor reduces the voltage and current changes.

The MOSFET switches more slowly. The capacitive parasitic turn-on may be obviated by reducing the R_{Goff} value, leading to better coupling to ground to throw the gate driver loop.

6.3.2 Separate gate resistors to achieve non-critical turn-on and turn-off

In many applications non-critical switching characteristics may be achieved when separate turn-on and turn-off resistors are used. Choosing $R_{Goff} < R_{Gon}$ prevents a capacitive turn-on via the Miller capacitance (see section 6.2 “Turn-on via the Miller capacitance”).

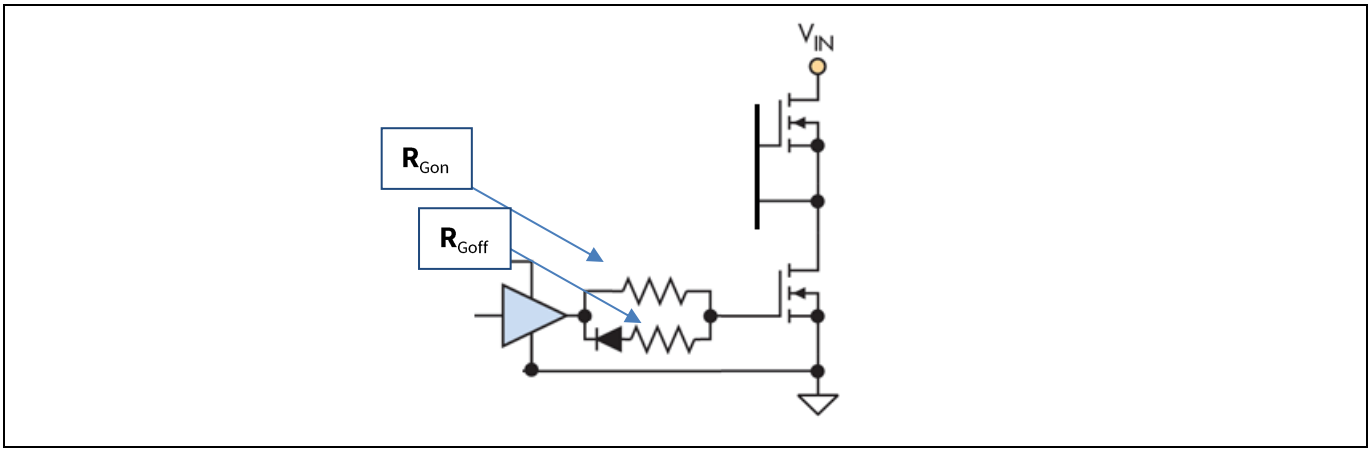


Figure 25 Separate turn-on and turn-off resistors

6.3.3 Additional gate emitter capacitor to shunt the Miller current

The switching behavior may be influenced with an additional capacitor C_{GS} between gate and source. The capacitor is there to take up additional charge originating from the Miller capacitance. Due to the fact that the total input capacitance of the MOSFET is $C_{iss} = C_{GD} + C_{GS}$, the gate charge necessary to reach the threshold voltage is increased.

Due to the additional capacitor the required driver power is increased and the MOSFET shows higher switching losses depending on how the $R_{Gon/off}$ is modified.

Table 4 Effectiveness of different measures

Measure	Turn-on due to the Miller capacitance	Switching losses
Reducing $R_{Gon/off}$ (one R_G design)	+	↓
Increasing $R_{Gon/off}$ (one R_G design)	-	↑
Additional C_{GS}	+	↑
Reducing R_{Goff}	+	↓
Reducing R_{Gon}	-	↓
Increasing R_{Goff}	-	↑
Increasing R_{Gon}	+	↑
Additional C_{DS}	+	↑

Note: + : Improvement - : Deterioration ↑ : Increase ↓ : Decrease

Note: Whenever the internal parasitics (C_{GD} and C_{DS}) of the MOSFET are low, it may become necessary to use an external capacitor C_{DS} to ensure a reduced dv/dt. The external capacitors are in the range of 10 pF to 100 pF and give the designer a fixed value with which to design for these parasitic capacitances.

7 Measurements

The double-layer BLDC 100 W demo board was tested driving a BLDC fan motor using FOC. The temperature steady-state was reached before reading the temperature on the CoolMOS™devices. After the measurement the load is increased by 10 W input power P_{AC}. For details about measurement equipment, see Table 5.

Table 5 Equipment list measurement parameters

Name	Comment
BLDC fan motor	
Power	110 W
Power factor	0.81
Number of poles	4 pole pairs
Phase resistance	27 Ω
Phase inductance	103.6 mH
Maximum speed	1800 RPM
Phases connection (U, V, W, N)	Star connection
Yokogawa WT3000 power analyzer	
Voltage range	600 V
Current range	2 A
Line filter	50 Hz
Output three-phase wirings	3P4W
Input one-phase wirings	1P1W
Temperature measuring equipment	
Thermocouples	J-type GG-JI-36-SLE
Temperature measuring unit	A55003830
Thermal camera	FLIR

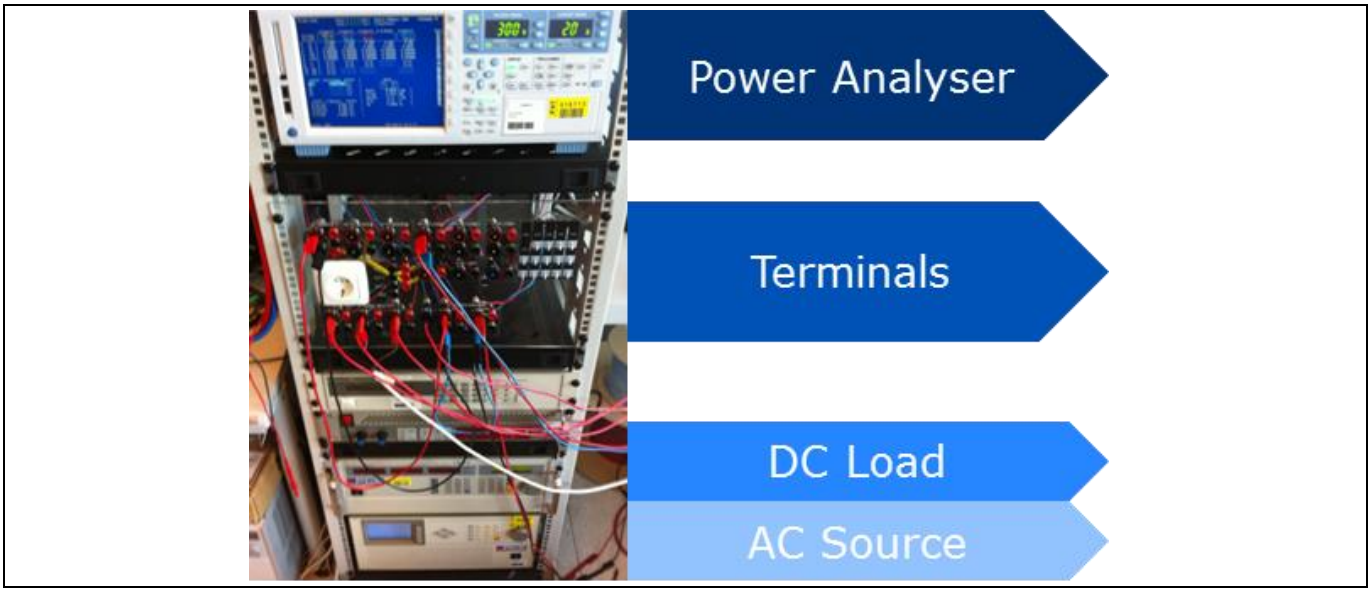


Figure 26 Measuring equipment

7.1 Test set-up

The EVAL_100W_DRIVE_CFD2 board was tested on a test bench developed by Infineon used to simulate a real cooling fan application. The board is designed for a 100 W output and consists of an input rectifier stage and an inverter stage. The CoolMOS™devices are driven by a 600 V gate driver IC from Infineon (2EDL05N06PF) and the modulation pattern is provided by an Infineon microcontroller (XMC1300) mounted on the same board. No heatsink is required, just thermal vias through the PCB. The control method is sensorless FOC using a shunt-based feedBack loop. The board is driving a 100 W BLDC fan motor. The efficiency is monitored by a Yokogawa WT3000 power meter and the case temperature is monitored by an infrared camera.

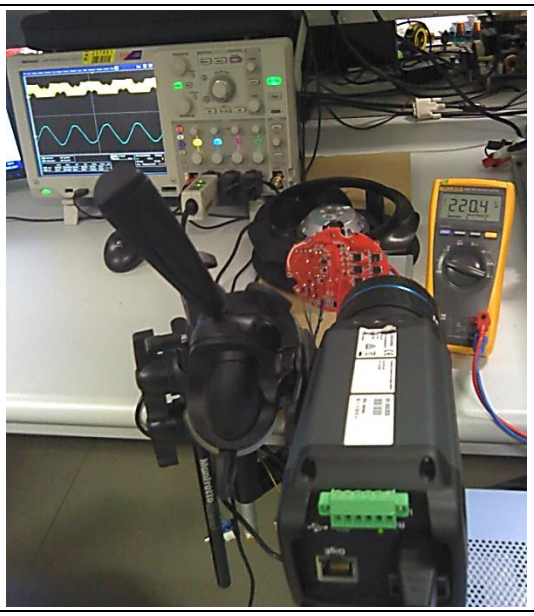


Figure 27 Test set-up for the application measurements

7.2 Thermal behavior

The temperature distribution is quite uniform, as demonstrated by detailed analysis of the thermal images:

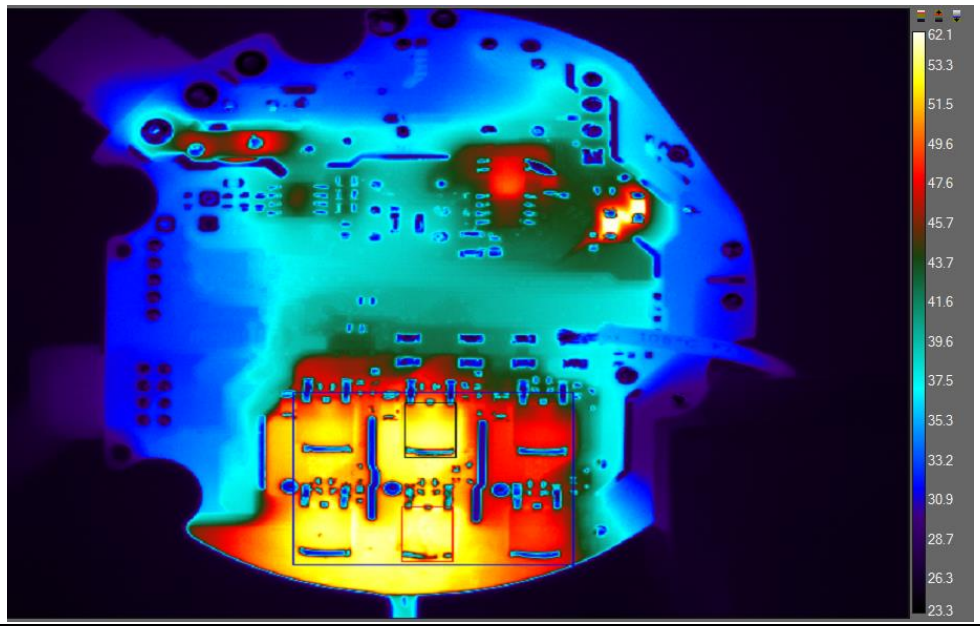


Figure 28 Thermal images at P_{in} = 50 W, $f_{_sw}$ = 15 kHz, T_{max} = 62.1°C

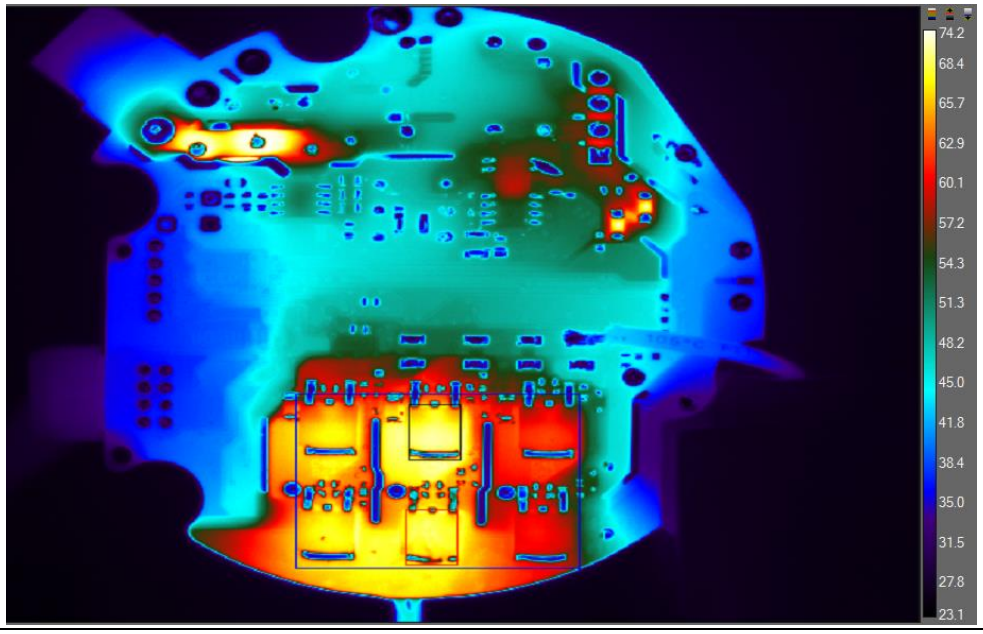


Figure 29 Thermal images at P_{in} = 100 W, $f_{_sw}$ = 15 kHz, T_{max} = 74.2°C

7.3 Conducted EMI

The conducted EMI has been measured on the EVAL_100W_DRIVE_CFD2 at full load. The measurements are shown in Figure 30 and Figure 31 for 230 V inputs. In the figures both peak (blue) and average (red) measurements are shown, together with the corresponding EN 55022 standard class B limit.

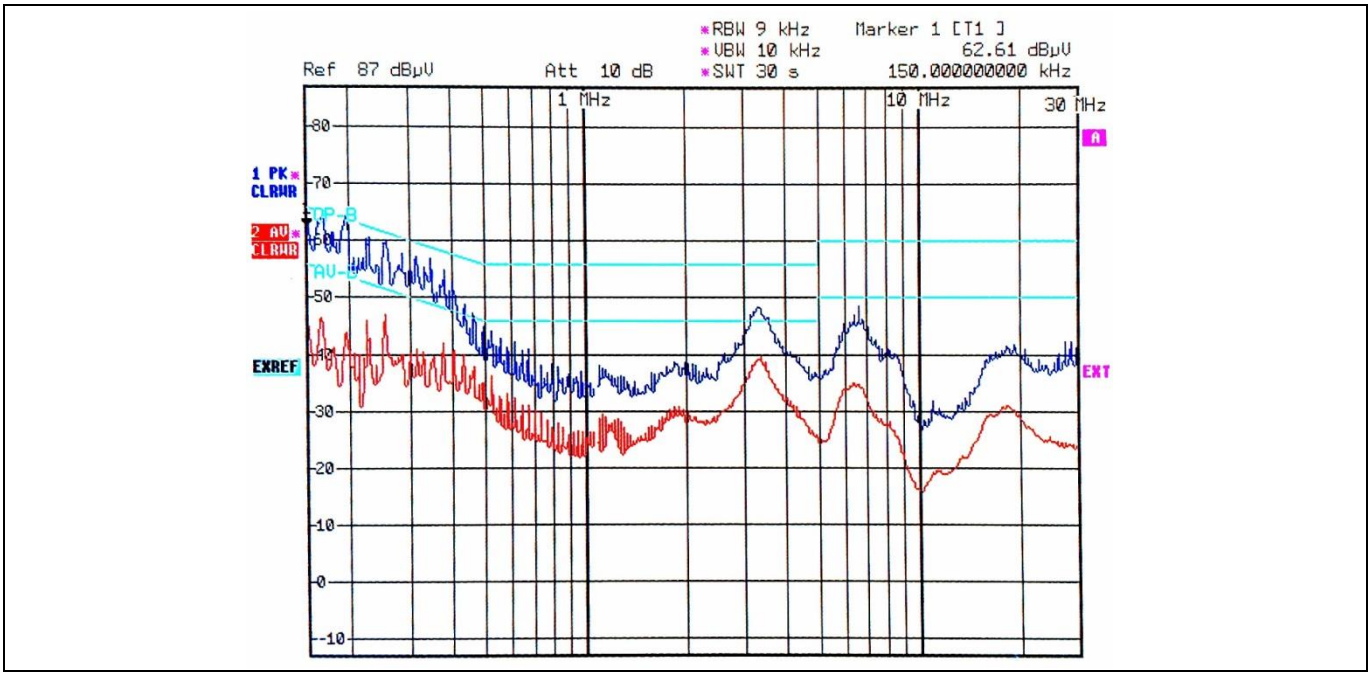


Figure 30 Conducted EMI measurement of the board at 100 W full load

If users wish to have a 10 dB EMI safety margin, this can be achieved by increasing the EMI input filter choke from 2.2 mH to 18 mH, affecting the EMI measurements as shown in Figure 28.

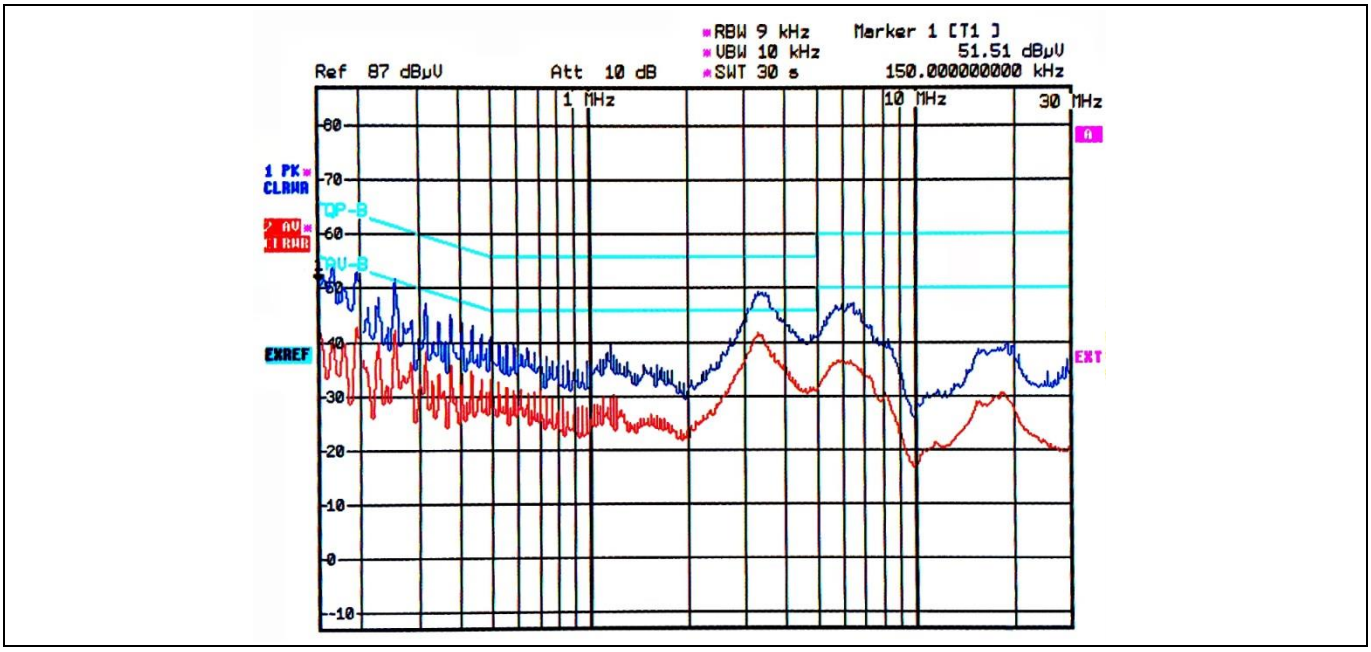


Figure 31 Peak (blue) and average (red) conducted EMI measured at full load and 230 V input

7.4 Efficiency

The test was performed with 220 V AC up to 100 W load, with an ambient temperature of 25°C and the switching frequency at 15 kHz. Besides the losses of the power switching the efficiency includes the rectification, driving and power supply losses. The complete board efficiency results are shown in Table 6.

Table 6 Efficiency measurement, f_{sw} = 15 kHz, IPD65R650CE

P_{DC} [W]	Phase I_{DC} [Arms]	I_{AC} [Arms]	Efficiency [%]
30	0.11	0.30	89.41
45	0.18	0.44	91.79
55	0.21	0.54	92.4
65	0.25	0.64	92.92
75	0.29	0.72	93.22
85	0.33	0.81	93.47
100	0.39	0.96	93.7

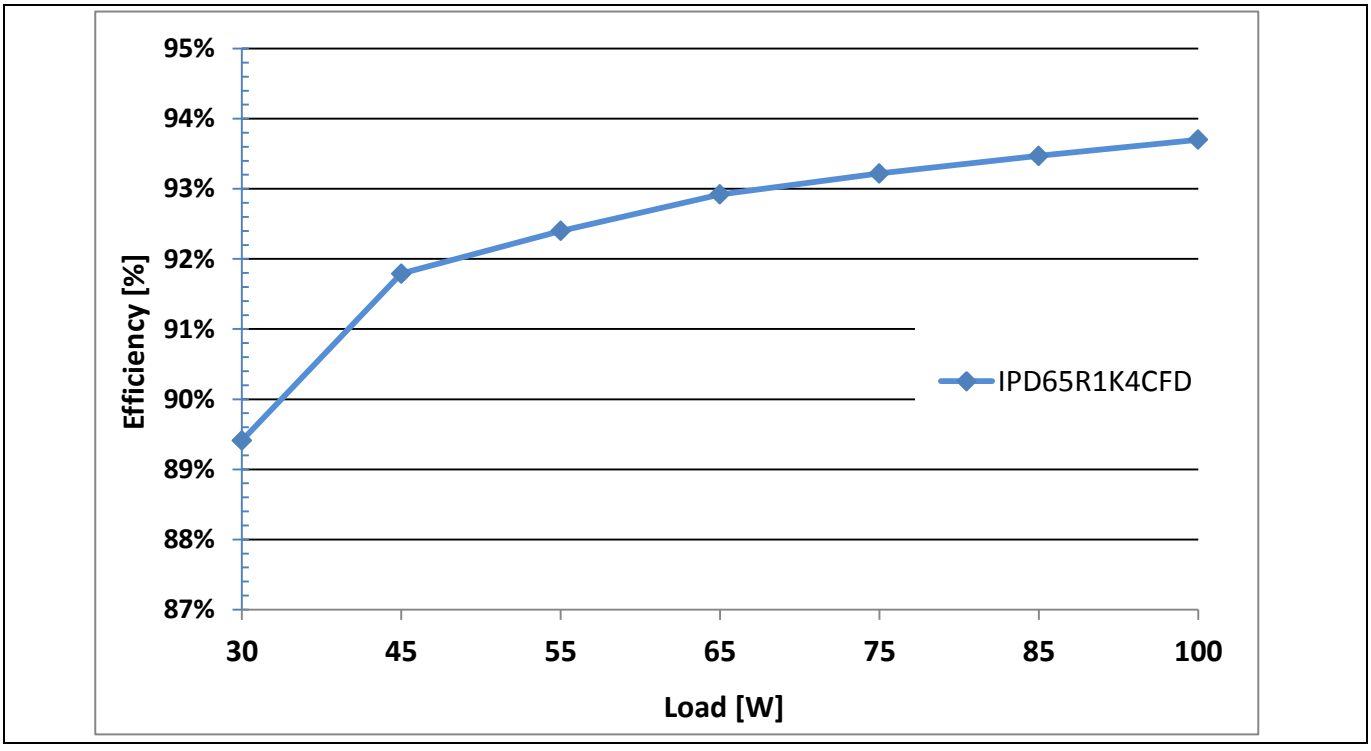


Figure 32 Efficiency measurement curve f_{sw} = 15 kHz, IPD65R1K4CFD

8 Board information

8.1 Board layout

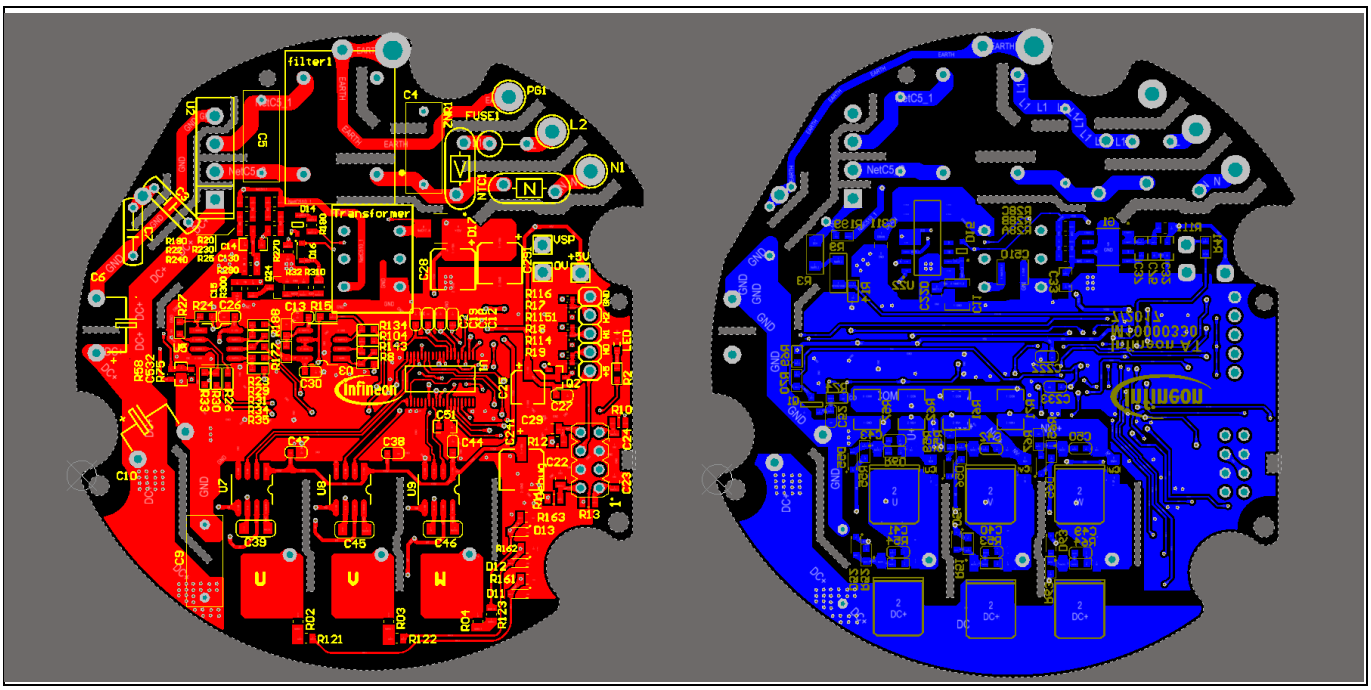


Figure 33 Board layout top view (left) and bottom view (right)

9 Useful materials and links

More information: www.infineon.com/CFD2

650V CoolMOS™ CFD2

Balance between efficiency and robustness with fast body diode



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A recent trend in high power conversion is the move toward higher and higher power density. High power density can be achieved best by resonant switching topologies such as zero voltage or zero current switching, which enable higher efficiency by eliminating the turn-on losses.

Key features	Key benefits	Applications
• First 650V technology with integrated fast body diode on the market • Limited voltage overshoot during hard commutation • Significant Qg reduction compared to 600V CFD technology • Tighter $R_{DS(on)}$ max to $R_{DS(on)}$ typ window • Easy to design-in • Lower price compared to 600V CFD technology	• Low switching losses due to low Q_{rr} at repetitive commutation on body diode • Self limiting di/dt and dv/dt • Low Q_{oss} • Reduced turn-on / turn-off delay times • Outstanding CoolMOS™ quality	• Telecom • Server • Battery charging • Solar • HID lamp ballast • Motor drives

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Perfect match!
EiceDRIVER™ 1EDN and 2EDN gate driver for MOSFETs

MOSFET Finder
Select Breakdown Voltage
I_D (max) ≥ 5 A
$R_{DS(on)}$ (max) < mΩ
ATV IND Any
Reset Find >

10 Board schematics

Figure 34 Microcontroller

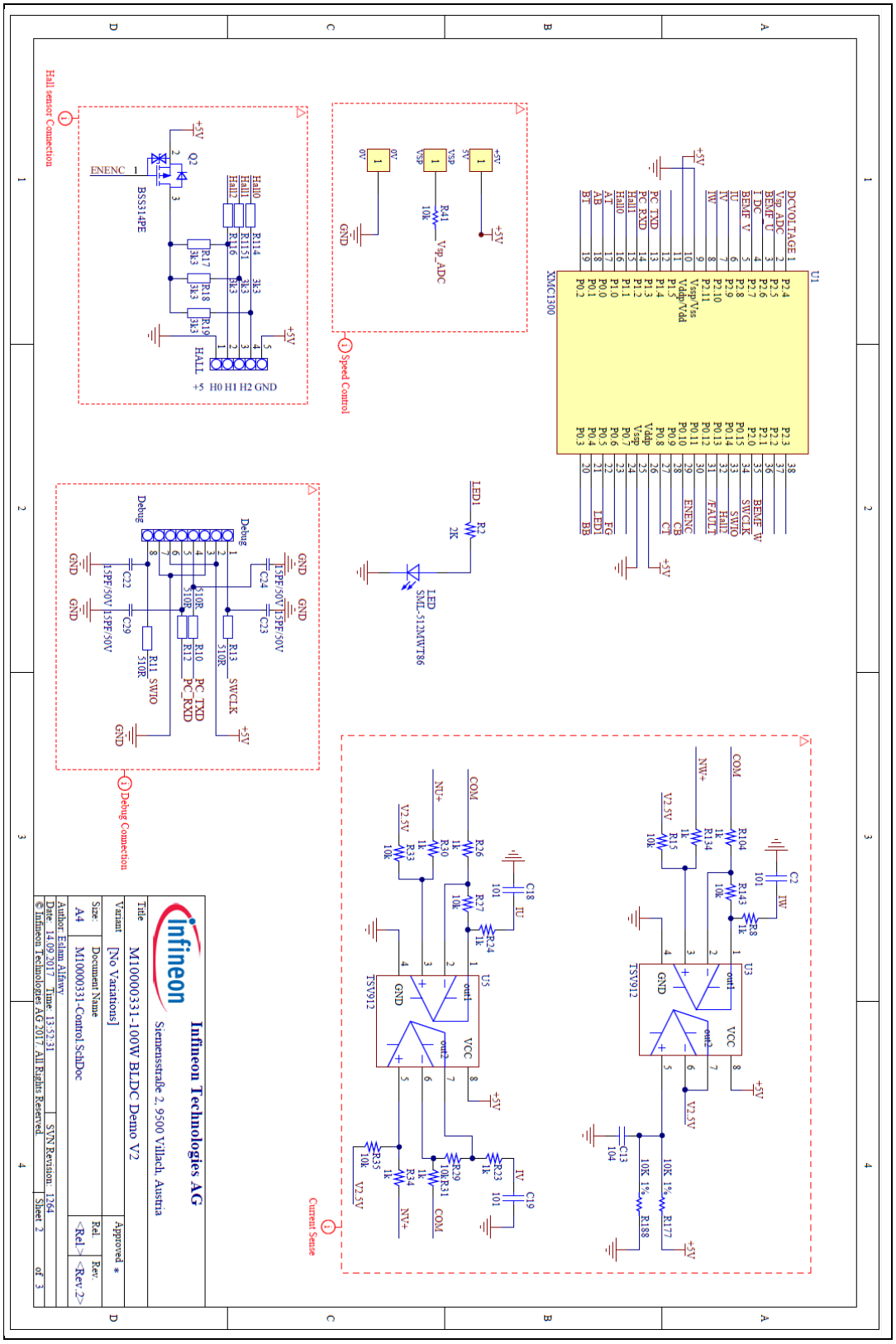


Figure 35 Power section

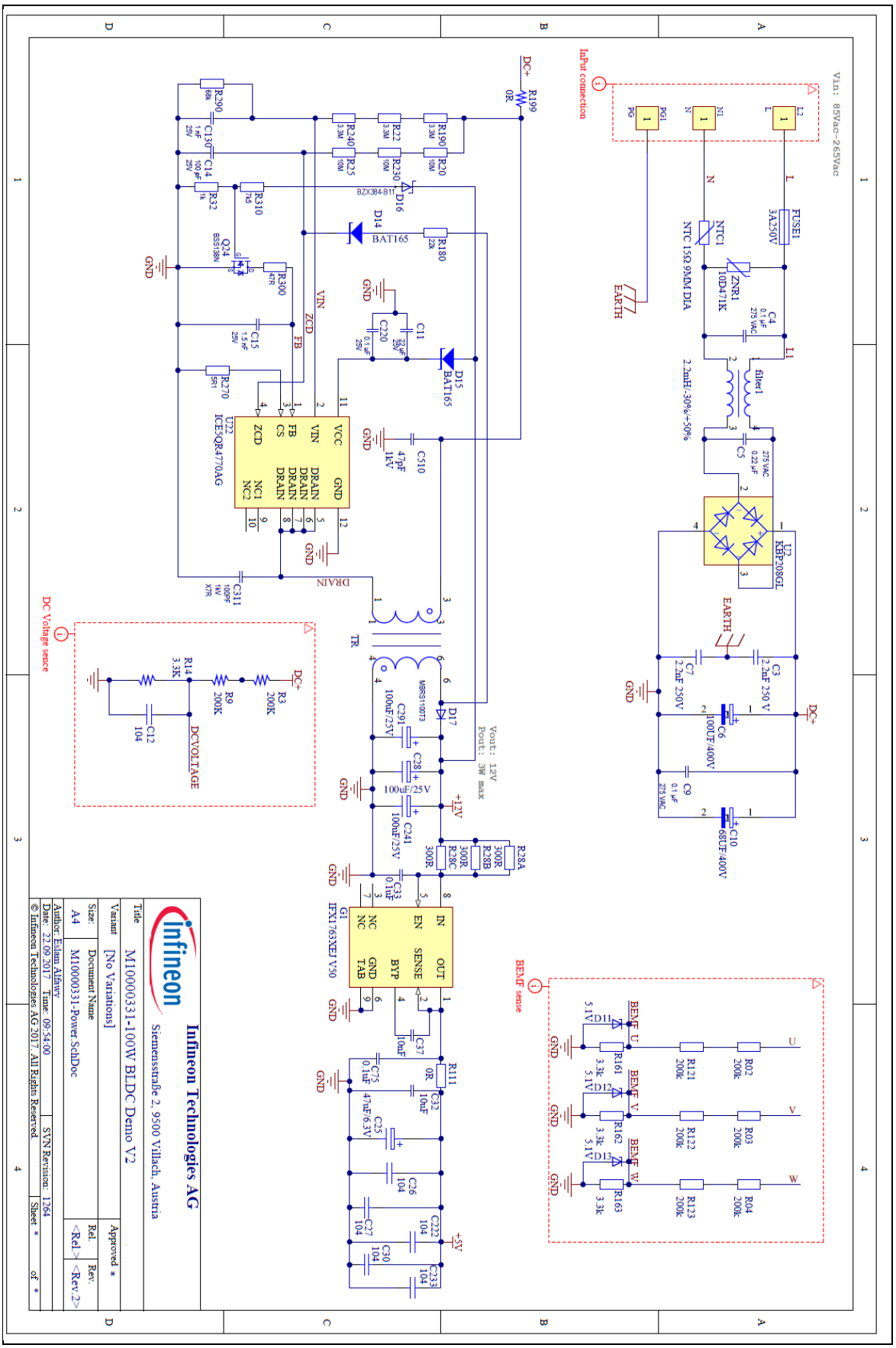
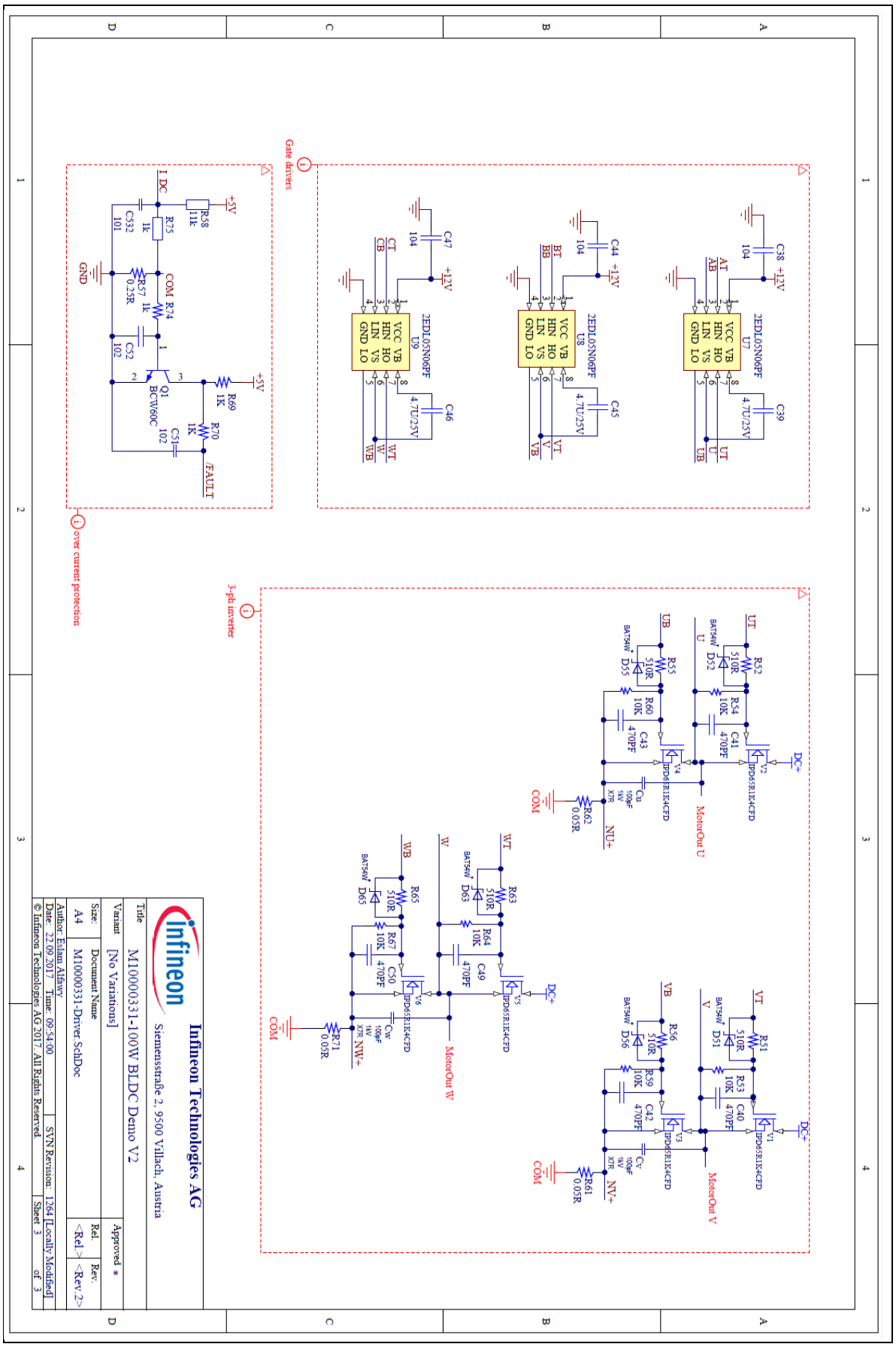


Figure 36 Inverter section



11 Bill of material

No.	Ref.	Description	Package	Manufacturer
1	V1, V2, V3, V4,V5, V6	IPD65R1k4CFD	TO-252AA	Infineon
2	G1	IFX1763XEJ V50	SO-8	Infineon
3	U1	XMC1302_TSSOP38	TSSOP38	Infineon
4	Q2	BSS314PE	SOT323	Infineon
5	U7, U8, U9	2EDL05N06PF	SO-8	Infineon
6	U22	ICE5QR4770AG	DSO12	Infineon
7	Q24	BSS138N	SOT323	Infineon
8	D14,D15	BAT165	SOD323	Infineon
9	D52,D55,D51,D56,D63,D65	BAT54W	SOD323	Infineon
10	Q1	BCW60C	SOD323	NXP
11	U3, U5	TSV912	SO-8	ST
12	FUSE1	3A-250V	0034.6019	SCHURTER
13	LED	LED	SMD0603	Any
14	NTC1	NTC 15Ω 9MM DIA	B57153S0150M000	EPCOS
15	ZNR1	VARISTOR	MOV-10D471KTR	BOURNS
16	TR	7491181012	Off-line transformer	WURTH ELE
17	U2	KBP208GL	800V, 2A KBP, 4-Pin	Diode Bridge
18	Filter1	PLA10AN1522R0R2B	1.5mH, 2A, Baureihe PLA10	MURATA
19	C2, C18, C19,C532,C14	Capacitor Ceramic 100pF/25v	SMD 0603	Any
20	C3, C7	2,2nF 250 V	Ceramic Capacitor	Any
21	C4, C5, C9	0.1uF/ 275 VAC	890324023023	WURTH ELEKTRONIK
22	C6	100UF/400V	400KXW100MEFC16X30	Rubycon
23	C10	68UF/400V	400KXW68MEFC12.5X40	Rubycon
24	C12, C13, C26, C27, C30, C38, C44, C47, C222, C233,C220,C33, C75	0.1 Uf/25 V	SMD 0603	Any
25	C22, C23, C24, C29	15PF/25V	SMD 0603	Any
26	C25	47uF/6.3V	SMD	Panasonic
27	C28, C291	100uF/25V	SMD	Panasonic
28	C32	10uF/25v	SMD 0603	Any
29	C37	10nF/25v	SMD 0603	Any
30	CU,CV,CW,C311	100PF/1KV	SMD 1206	Any
31	C39, C45, C46	4.7uF/25V	SMD 1206	Any
32	C40, C41, C42, C43, C49,	470pF/25V	SMD 0603	Any

	C50			
33	C51,C52,C130	1nF/25V	SMD 0603	Any
34	C241	220uF/25V	SMD	Any
35	C11	22uF/25V	SMD 1210	Any
36	C15	1.5nF/25V	SMD 0603	Any
37	C510	47pF/1kv	SMD 1206	Any
38	D17	MBRS1100T3	SMB	Any
39	D16	BZX384-B11	SOD323	Nexperia
40	D11, D12, D13	MM3Z5V1ST1G -5.1V	SMA_SUB	ON SEMICONDUCTOR
41	R2	2K	SMD 0603	Any
42	R02, R03, R04, R121, R122, R123	200k	SMD 0603	Any
43	R3, R9	200k	SMD 1206	Any
44	R8, R23, R24, R26, R30, R31, R34, R69, R70, R74, R104, R134,R75,R32	1k	SMD 0603	Any
45	R10, R11, R12, R13,R51, R52, R55, R56, R63, R65	510R	SMD 0603	Any
46	R15, R27, R29, R33, R35, R41, R53, R54, R59, R60, R64, R67, R143,R177, R188	10k	SMD 0603	Any
47	R17, R18, R19, R114, R116, R1151,R14,R161, R162, R163	3.3K	SMD 0603	Any
48	R28A, R28B, R28C	300R	SMD 0603	Any
49	R58	11k	SMD 0603	Any
50	R199,R111	0R	SMD 0603	Any
51	R20,R230,R25	10M	SMD 0603	Any
52	R190,R22,R240	3.3M	SMD 0603	Any
53	R180	22K	SMD 0603	Any
54	R290	68K	SMD 0603	Any
55	R310	7K5	SMD 0603	Any
56	R300	47R	SMD 0603	Any
57	R270	5R1	SMD 0603	Any
58	R61, R62, R71	0.05R ±1%	R-sense SMD1206	Any
59	R57	0.25R ±1%	R-sense SMD1206	Any

Revision history

Document version	Date of release	Description of changes

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